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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: John WOOD

Title: IMPEDANCE MODULATION SIGNALLING

Appl. No.: 09/613,588

Filing Date: July 10, 2000

Examiner: Unassigned

Art Unit: 2731

CLAIM FOR CONVENTION PRIORITY

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

The benefit of the filing date of the following prior foreign application filed in the following foreign country is hereby requested, and the right of priority provided in 35 U.S.C. § 119 is hereby claimed.

In support of this claim, filed herewith is a certified copy of said original foreign application:

- United Kingdom Patent Application No. 9800440.1 filed January 10, 1998.

Respectfully submitted,

Date SEP 27 2000

By _____

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Cardiff Road
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1. Your reference MIRRORMODE

2. Patent application number *(The Patent Office will fill in this part)* 10 JAN 1998 9800440.1

3. Full name, address and postcode of the or of each applicant *(underline all surnames)*

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Patents ADP number *(if you know it)*

If the applicant is a corporate body, give the country/state of its incorporation

4. Title of the invention DIGITAL REFLECTION INTERNET

5. Name of your agent *(if you have one)*

"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*

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9/77
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6. If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and *(if you know it)* the or each application number

Country	Priority application number *(if you know it)*	Date of filing *(day / month / year)*

7. If this application is divided or otherwise derived from an earlier UK application, give the number and the filing date of the earlier application

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Any other documents *(please specify)*	

11. I/~~We~~ request the grant of a patent on the basis of this application.

Signature [signature] Date 9/1/97

12. Name and daytime telephone number of person to contact in the United Kingdom JOHN WOOD 01933 418388

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7/1/97

DIGITAL REFLECTION INTERNET

Method for Digital Signal (combined with Electrical Power) Transmission and Distribution

The invention relates to a method for high speed digital signal transmission and distribution. The system principally suits electromagnetic waves in electrical transmission lines (e.g. Copper Coax, Twisted pair) but is also applicable to optical (fibre optic) communications. The invention facilitates transmit and routing electrical power (DC or AC) on the same cabling (for copper mode)

The system is entirely general purpose and can be applied anywhere digital signals are used. The list of applications are too numerous to mention, a few examples are:- Computer Backplanes (BUS), Digital information networks (Internet, PC Office networks), Intelligent peripherals and actuators (E.g. Printers, Plotters), Digitising sensors (Temperature, force sensors).

The system solves most of the major problems encountered in high speed digital signal distribution. These problems are:-

- Problems of High speed Clock distribution
- Difficulty and complication in addressing individual components on a distributed bus
- Complication involved in routing digital transmissions between destinations
- Problems of spurious reflected waves on transmission lines
- Complexity and expense of implementing error detection and correction
- Cable attenuation of fast electrical signals on long runs (has adaptive speed)

The invention uses circuitry to induce reflections (stop signal propagation) in a controlled way to achieve two-way (bi-directional) digital communication between one or more physically separated but electrically or optically interconnected units.

The system is capable of implementing many architectural schemes for network topology but for sake of examples the descriptions here will focus on the common situations where one 'Master' unit can communicated with one or many 'Slave' devices and on a Interconnected network (Internet) type arrangement. Most of the terminology used relates to Network jargon, but for each term there exists a matching term for computer backplane (multi-bit buses).

The conventional approach to implementing a Master / Slave system is well known and involves designating a unique 'address' (or address ranges) or 'serial number' to each device attached to the bus.
Digital electrical signals are formatted either in time (serial network) or into a binary multiwire bus (computer backplane) so as to make an addressing scheme. All attached nodes receive the same 'packet' of data but only the node with the matching address code will respond. The response could be to accept some digital data from the Master or send out some digital data to the master depending on the protocol. By sequencing through the addresses of the attached nodes, the Master unit (usually a computer) can implement a control function for the total system as determined by software. The main problem with such an addressing scheme is that unique addresses need to be embedded in devices and that any device wishing to attach and participate in a network needs to be aware of the address of the nodes to which it is to operate with.

In recent years, in large systems (such as office computer networks) there has been a move away from multipoint 'tap-in' "Ring topology" networks systems in favour of Point-Point "Star" data links with 'hubs' and 'repeaters' to route and amplify signals. The reason for this is that at the higher and higher data rates required for modern computers normally produce too many spurious signal reflections on the transmission line medium at high speeds. This is to the annoyance of many small network operators where the convenience of a 'tap in' to a "Ring" topology offered an easy way to expand a network without the need to add more wiring or buy expensive intelligent hubs and repeaters.

General observations on Transmission line phenomenon

Transmission lines will propagate electromagnetic waves with a characteristic speed (some fraction of the speed of light) and with a characteristic wave impedance (X ohms) and that this energy will propagate free of reflections only when the transmission line has uniform impedance and is infinite or else terminated in a resistance equivalent to the characteristic impedance (refer to Figure 1)

Whenever an electrical transmission line is improperly terminated (that is with an impedance higher or lower than it's characteristic impedance) some portion of the incident wave energy will not be absorbed and must therefore be reflected back in the opposite direction on the cable. This is well known in RF engineering and a figure of VSWR (Voltage to Standing Wave Ratio) is often applied to give an indication of the mismatch. Optical systems are also subject to reflections caused by a change in wave impedance for these systems it is usual to speak in terms of Refractive Index rather than wave impedance

The two theoretical extremes of mismatch are (1) a short circuit termination [Zero resistance] (2) an open circuit termination [infinite resistance]. Both of these cases are approximated (relative to typical transmission line impedences) in real situations.

Referring to the diagrams (and assuming loss free perfect cables),
An Open Circuit transmission line's response to a transmitted wave is shown first. During propagation, the signal in the cable stays at the level as was shown at the entry to the cable. When the wave reaches the end of the transmission line however, the voltage detected by an oscilloscope would show a pulse of twice the magnitude as was measured at the coax entry point. This is because what is being measured is the incident wave arriving at the end of the coax (normal magnitude) plus the reflected wave voltage of similar magnitude - the wave front has nowhere to go so the stored electromagnetic energy in the incident wave ramps the voltage up the additional amount on top of the instantaneous voltage of the incident wave - if the incident wave voltage could somehow be removed from the reading it would be clear that the reflected wave was the same wave as arrived, same magnitude and same phase.

A short circuit transmission line response is shown below. With the same wave put into the cable, transmission proceeds as normal (wavefront driving the characteristic impedance of the cable) until the leading edge of the wave meets the short circuit. An oscilloscope probe will obviously see no signal on the short circuited line but the incident wave does produce a current (e.g. by ohms law a 50 ohm line with a 5volt signal will produce a 100mA current through the short circuit path). Doing the logic in reverse, the current produced by the short circuit of the incident wave is exactly the right value when multiplied by the characteristic impedance to produce a voltage wave which cancels the incident wave voltage - this effectively what is happening with the electromagnetic energy in the cable. This 'cancellation' wavefront doesn't stay at the short circuit but moves with

back towards the transmitter end of the cable like any conventional signal. Actually, if the system was observed beginning from the time when all the incident pulse had been fully reflected (no trace of it left anywhere on the cable), it would appear that a pulse was being sent by the reflection end toward the transmission end.

The fundamental difference between the Open Circuit and Short Circuit reflection is that in the first case, the returned signal is In-Phase reproduction of the incident signal whereas in the second case the returned signal is an Inverted (Anti-phase) copy of the incident waveform. This well known effect is one of the basis for the invention.

Description of Invention by way of an example embodiments
[Continuing with the example of a Copper cable and Master / Slave]

BASIC SYSTEM (Single Master, Multiple slaves) See FIG 3
- The Master unit is the source and destination in all data transfers
- Data transfers take place via electrical pulses through Coax or twisted pair transmission medium [could be optical pulses on fibre optic medium]
- System **does not** require addresses or serial numbers for unique addressing of each item on the bus.
- All critical timing functions (as affect performance) are performed by the Master electronics.
- Nodes are connected in series. [Sometimes called a "Ring" or "Daisy Chain" topology]
- DC electrical power (or low frequency AC) is furnished along with the two-way data transfer medium.

Master:-
Component parts:-

- Programmable clock bit rate (3x rate clock)
- Serial Data output
- Serial Data input
- Output terminating resistor (Same resistance as characteristic impedance as Coax)
- Virtual "Hybrid" network.
- "Three level" output data pulse generation and reception + Pulse Quality checker

The actual electronic circuits in the logic blocks can be can be implemented with conventional well known integrated IC techniques.

Virtual "Hybrid" network.
This performs the same operation as the Transformer Hybrid coupler in the early telephone sets i.e. 4 wire to 2 wire conversion. As applied here it is able to separate the Master output waveform (Transmitted data) from the reflection signals coming back to the Master from the reflective nodes.
Operation:-
- The differential amplifier gives an output corresponding to the difference in voltage between its inputs. Without any reflections arriving back at the coax, the voltage divider effect between R and the coax impedance produces a 2:1 voltage division. R1 and R2 are equal value and also produce a the same 2:1 voltage division. So, with no reflections arriving, the differential amplifier sees the

same signal whatever the master signal driving the line (Diff amplifier has identical inputs of equal magnitude and phase) and so gives no output. However, whenever reflected energy arrives back at the master, the voltage at the coax centre conductor will increase or decrease by some voltage. This voltage is not present on the R1:R2 voltage divider and so the differential amplifier will output the difference. In principle, this gives a signal of only the reflected (incoming) components of voltage - the output signal having being removed.

Signalling Method

- Signals used are short symmetrical pulses. They have no DC component to allow for entirely AC coupling used throughout. Refer to FIG2 diagram showing symmetrical "sine like" shape. A binary logic '1' is encoded by generating a pulse first +Ve then -Ve. A binary logic '0' is encoded by sending the line first -Ve then +Ve. A gap period is inserted after the pulse to allow for time to interpret the pulse. These pulses are later referred to as waves or wave pulses in the following notes.

"Three level" output data pulse generation SEE FIG 5

- Preferred method of signalling is with a three level system. This is inherently less fast than a NRZ (non return to zero) binary code (which could however be used) but offers advantages of symmetry and ease of decoding and error checking. Three level digital systems are in common use in telephony but do not have the waveshape or the encoding chosen here (Symmetrical with time and amplitude).

- Note that the third-state used as an output here is not a High Impedance "off" state (As is commonly seen in Tri-State™ logic gates used for Bus isolation) but a low-impedance voltage state mid-way between the '0' and the '1' levels.
- Most of the other digital circuitry operates on conventional two-level binary logic.
- The third state, when encountered on the transmission medium shall be termed a "Gap" period in the notes which follow. It represents an absence of signal and in this sense it will be used to control some aspects the operation of the addressing scheme. The gap can be generated by the Master or the Slave depending on which was supposed to be active at the particular time.
- Wave shaping on the output waveform reduces generated EMI radiation. The waveshape should be perfectly balanced (ideally) because as one option, this symmetry can be tested to give confidence
in the integrity of the data pulse (on a pulse by pulse basis).

Pulse Quality checker – SEE FIG 4

This system can detect errors in each single bit of data transferred with very good dependability.

The receive waveforms are by design of the same type and shape as transmitted (see later). For the binary codes '0' or '1' to be accepted a sequence of checks is performed to ensure that the data received was valid.
For binary '0' and '1' the following tests must pass:-
- Firstly, the waveform must be preceded by a period of gap (at least the inter-bit gap). This will detect framing errors and general noise on the lines preventing a stable zero reference.
- Second, the waveform must first exceed either the +Ve or -Ve threshold. This check, together with a 'false' reading from the gap detect (finding that isn't gap) picks up signals which are too weak (between gap and logic thresholds)

- Third, the waveform must go on to invert and exceed the opposite threshold within a time period set by the Master unit. This prevents a single glitch of noise from being interpreted as data since it is very unlikely that a noise pulse could be first +Ve then -Ve during the sampling period without it being of very similar frequency and double amplitude to cancel any valid signal.
- Forth, when the gap is again detected after the two polarities of pulses as mentioned above, the integrated total of +Ve and -Ve currents must balance within a fixed percentage. This test is performed by the integrator shown in the block diagram (actually could be just a transistor with capacitive Collector-Base feedback). Any unipolar noise pulse occurring during the sample time would leave the integrator with a net non-zero output whereas a pure reflection of the symmetrical (wave-shaped) output data stream will give close to zero amount of imbalance. [except for long distance transmission spurious reflections. see later on Reflection rejection memory]. This check verifies the symmetry of the waveform. A diode limited clamp produces an inverse log response to cope with wide range of returned signal strengths.

The above tests give an error output for the following conditions:-
- receive signal too weak
- common mode noise voltage detected

Note that fixed threshold levels are shown. It might be advantageous to employ DAC converters to allow adjustment of these levels in software to facilitate communication with a wide range of round-trip signal attenuation levels. Also not shown but possible is to apply DAC adjustable response time control of the receive comparators and amplifiers to reject HF noise when operating at low data rates (as might be required for reliable communication with distant nodes). Adjustment of time constant can be achieved by DAC setting of the bias currents in these components - larger currents giving faster response with fixed parasitic or added capacitances.

The gap period must persist for a given amount of time before the previous data is accepted. This way noise will be detected at the gap time

Gap / Strobe / Reset

The "quiet" or gap period on the bus can have meanings assigned to it depending on how long it lasts. The gap is detected when the Three state level detector comparators signal that the voltage is within a certain range of zero AC volts.
- A gap of more than a certain length of time can be interpreted as a Strobe pulse.
- Gap much more than the strobe time threshold can be interpreted as Reset time.
(More descriptions of these conditions will be given later)

Data rate establishment

- System can (in theory) run always at the maximum data rate available to the nodes and cabling.
- System capable of changing data rates on a bit by bit basis by changing the clock divider.
- To establish the operating speed as a one-time configuration sequence Master can for each node send data at higher and higher speed until cable attenuation (a variable depending on distance and cable quality) result in the returned reflection signals failing to meet quality standards [attenuation increases with frequency]. Master then in future always operates nodes at less than this data rate. Process can be run again if additional cabling is inserted between nodes or conversely if sections of network cable are upgraded to higher quality media.

Slave node (basic):- (FIG 6)

Reflects on a pulse by pulse basis. Can reflect as Short Circuit or Open Circuit with the electronics shown.

The echo acts as an acknowledgement by the node of the data. The quality detector at the Master can determine if the echo signal had been corrupted. It is very difficult for any external noise source to corrupt a reflected '0' into a '1' and pass the quality tests.

Since the Master is the source of all waveforms and the nodes are only required to reflect these pulses, the wave shaping on the master output pulses is also present on the return reflections.

Component parts
- Transformer
- Three level logic detection
- Short circuit reflector / Detector #1
- Short circuit reflector #2
- Current source transistor
-

Transformer FIG 7 FIG 8

- This is a wideband pulse transformer. Preferred construction would be as an inverting transmission line transformer made from either coax or twisted pair wound around a high permeability torroid core. Designs for these are well known. Another alternative would be to fabricate a Microstrip transmission line transformer on a PCB and use Planar magnetic cores (available from Phillips) to magnetically link the circuits.
- Use of transmission line transformer allows good DC path with low parasitic elements (transmission line construction effectively makes stray capacitance and leakage inductance become the transmission line).
- The transformer can also with advantage be arranged to perform impedance conversion and single-double ended conversion (Balun function). This would be useful for converting the signalling medium between Coax (unbalanced) and Twisted pair (balanced) cabling systems.

Inherent inversion of the through data (both ways) need not cause a problem because the Master can easily invert all it's output data for alternate nodes it talks to. Similarly, the receive data will alternate in sense for odd and even numbered nodes and this too can be inverted in software (not actually required when compared to sense of wave transmitted — see later notes).

(Semiconductor options) FIG9

NOTE:- a transformer is not the only conceivable method of linking two RF ports with either High or low impedance RF path. A power Mosfet or NPN switch or other type of semiconductor or electromagnetic (e.g. relay) could be used to achieve this purpose. Systems which don't need a DC / lf AC electrical supply (e.g. where supply is already available) an entirely monolithic integrated system can be arranged using Pchannel or Nchannel mosfets as switches to connect or isolate one RF port from the other to induce "Open circuit" reflections or Through connection when required. Standard means of charge injection cancellation would limit spurious signals created during switching. Large size (power mosfets) devices could be used to allow good DC conduction path (see drawing).

Short circuit reflector / Detector FIG10

- The block diagram shows an analogue switch element with a series resistor. Actually the preferred circuit for this switch / detector is unconventional and a full circuit diagram is shown on a separate drawing.
- The circuit allows for the detection of the incoming waveform signal and simultaneous (short circuit) reflection of an incident wave

When the RF switch is off, the NPN emitter follower (TR1) is turned off. The base is reverse biased and the emitter current sink transistor (TR2) is also turned off by 0v on the base line. The emitter circuit plus collector TR2 represents a very high resistance in parallel with some small stray capacitance to ground. Rbias provides a reverse bias point and is typ >10Kohms. (The BIAS level of +2v is related through monolithic devices to the +2.6v mentioned below). When the RF switch is off, AC signals coupling via Ccupl experience very little attenuation or reflection since Rbias is a high resistance and TR1 emitter is reversed biased. In the off condition The switch can handle signals of 5 volt peak-peak before TR1 emitter becomes forward biased.

To turn the RF switch on, the switch control line goes to +2.6v. This very quickly turns on TR1 and slightly later, the current sink pair TR3,TR2. With correct timing it is possible to ensure that there is very little change in voltage at TR1's emitter (and therefore spurious output into Zsource) because the ultimate emitter voltage is also 2volt (2.6v-Vbe (typ 0.6v) = 2v). In the On condition,the emitter current of a bipolar transistor gives an effective output resistance of 25 / Ic (in mA) or 5 ohms at 5mA Ic. This is adequately low relative to Zsource to produce strong 'Short circuit' reflections of waves appearing at Zsource.

The switch is turned on or off only during the Gap time (see later) to limit spurious signal injection.

Rsense is added in TR1's collector so that an analogue of the Master signal (which appears as a modulation of emitter current) is available for the node to be able to receive the master data even when the wave is to be 'Short-circuit reflected' [the RF voltage Zsource and the Emitter are zero]

Short circuit reflector on Transformer mid-point

- This could be made similar to the previous design but because the on/off times are not critical for this switch (as will become evident later) a simple saturated NPN switch could be employed. This switch would conveniently pass DC current as might be required for Node / Actuator power.

Three level detection

- A more basic three level detection scheme can be implemented for the node. This is because all data pulses sent to the node during communication are reflected (in one way or another) back to the master where they can be tested for noise pickup (Quality checking). A simplifying, reasonable assumption made now is that if the round-trip pulse quality has been maintained then the one-way pulse quality to the node can be taken acceptable. On this basis, the simplest node needs no additional error detection and correction logic (plus it doesn't requiring clock generation nor addressing logic).

Current source transistor

- A saturated JFET or Mosfet or Bipolar transistor can be used to extract some operating current from the bus and still present a high AC impedance to signals on the bus. [This might also be incorporated into the Centre-tap transformer RF reflection switch as mentioned before.]

OR

Inductor

- For high power levels an RF inductor can be used to extract significant DC current for powering local electronics or actuators and still present a high AC impedance. Low frequency AC power is also possible (50Hz, 60Hz) as this is way below the normal signalling frequencies and so is isolated by the small coupling capacitors of the signalling circuits.

Operating principle of node

-Initially (Power on) Master output is the Quiet (Gap state). Assume this has persisted for longer than a Reset time period and so all nodes have been reset.
- Reset state primes all nodes for being addressable
[Refer to FIG6]
- Having been reset all nodes are set to reflect the first incoming wave with the short circuit reflector (RF switch #1) switched on to produce an Anti-Phase reflection.
- Master sends a wave to the node. For now it doesn't matter what the binary state of the Output wave is. Node reflects the wave Anti-Phase. This propagates back towards the master where it will be picked up using the pseudo-hybrid arrangement which separates the reflected wave from the outgoing transmitted waves which may be emitted continuously.
- Master can then continue now to send and receive data with the node at full duplex (see below)

Signalling Method continued

- Node receives a pulse either via the Sample point #1 or from Sample point #2. (Refer to FIG10 showing the preferred NPN RF reflector switch / detector circuit) Sample point #1 is used when the node is set to Anti-phase (Short circuit) reflect a wave since the RF switch would be on making a very small voltage detectable on Sample point #2. Sample point #2 is used when the node is set to In-phase reflect (Open circuit) the wave as in this case a large voltage (double the transmitted level) is present at this point.
- Signalling of data from the node back to the Master consists of turning on using the Antiphase (Short circuit) reflector RF switch #1 for a binary logic '0'. To send a logic '1' the node is set to reflect InPhase (Open circuit) reflection. This is achieved by having both RF switch #1 and RF switch #2 open circuit. An incident wave pulse from the Master appears at the node but the series inductance of the Wideband transformer (now acting as an inductor as can be seen from the winding polarity dots) presents a High impedance to the wave and so little energy is coupled through to the other port and on to other nodes [inductor current cannot instantaneously change and the waveshape of the Master generated pulses has very high frequency components only].
- For every bit of data received by the Node using the three-level detector to extract data (and a clock) one bit of Node data is returned to the Master. System can operate in a full-duplex mode. The reflector switches are only changed over during the quiet (Gap) time of Master pulses are so switch at zero voltage minimising spurious signal injection. It must be pointed out that always the node is set to either reflect Open Circuit or Short circuit and changeover only occurs during the Gap (zero volt) period. At no time can any signal pass the node being addressed and so nodes further down the line from the Master experience very little if any signals - they are reflectively isolated
- After each Master wave data pulse is received and shifted into the node, the next bit of node data to send back is clocked out of the Nodes shift register.

- Master receives exactly the same pulse back that it sent. Every pulse it sends out to the active node must be returned. By checking interpreted binary state of the received pulse as compared with the binary state of the same pulse when it was transmitted the master is able to determine the binary level of the bit which the node was sending. (If wave polarity is same then node did an In-phase reflection (Open circuit) so was sending a logic 1, if wave polarity is revered by the reflection (Short circuit Anti-Phase) then the node had sent a logic 0).
- Because it is fundamentally the same pulse used to transmit and receive the data, the quality checking back at the master on the returned signals confirms the absence of noise on the round-trip signal giving good indication of data integrity both ways.

Inherent Addressing mechanism

As described above, while ever a node is using reflections to send back all data pulse waves back to the Master, nodes further down the line cannot see any signal.

After a two-way data transfer is complete with a node (Arbitrary long), a special Strobe gap is inserted in the output stream of the master:-

Strobe (Short Gap, typ 500nS)

Strobe arises by detection of a communication gap from the master of greater than a certain time. This makes communication with the currently addressed node end. After detecting this strobe condition, the node simply doesn't reflect any more signals (Turns RF switch#1 off and RF #2 on)

The effect of RF switch#1 off and RF #2 on after strobe is detected makes the Wideband transformer act as true 1:1 inverting transformer and solidly couple the input and output RF ports in a bi-directional manner. This happens because the common point of the windings is switched to AC ground by RF reflector switch #2. This has the effect of coupling input RF energy present between winding terminal (1) and AC Ground(2) (energy from input port) via transformer action to the output of RF coax (winding terminal (4)). The transformer is inherently bi-directional and so couples signals originating at the right hand port back to the left hand coax port when RF reflector #2 is switched on.

RF switch #2 turning on therefore connects the RF ports (the coax cables) together for RF energy. This lets Master generated pulse waves pass by a node with this switch on onto the next node in the chain. Similarly, reflected energy from nodes past this 'switched out' node passes through back to the master. The inverting nature of the Transformer action causes a 180 degree phase reversal and consequent binary state reversal of waveforms for each node placed in a chain. This need not be a problem because the Master can easily alternate the polarity of it's transmitted data pulses for Odd numbered nodes.

[RF reflector switch #2 could be a saturated switching element of low resistance (NPN transistor) to also act as a path for the main DC current supply for the node. . Switching speed is not of the essence as it only needs to be switched on or off once per addressing cycle. In the non-saturated condition (constant current condition) it acts as a path for DC current but as high impedance for RF energy if the transistor has low collector capacitance.]

Strobe condition detected this way lets the Master quickly pass through all the nodes on the list to move to the one which it wishes to talk to. To do this, as it moves through the nodes it would

issue one data pulse (which gets reflected Anti-phase) followed by a Strobe gap period. This would be done until master was communicating to the node it wished to communicate with.

Once a node has been de-addressed by an Strobe detect, it cannot become an active reflector again until a Reset detect (mentioned later) re-arms the logic

[Node can also maybe instigate a similar signal back to the master (since communication is independent two-way) by not reflecting any data for a period during Master transmission. This can indicate that all required data from the node has been Taken / Given or, can be used as an early initial indication that an addressed node doesn't require data and so it is OK to move on to the next node in the chain.]

Reset detect (Long gap [typ 2uS])

A gap much longer than the strobe gap length from the Master indicates communication reset for a node. This resets only the communication logic of the node.

Reset detect re-arms a node to be able to be addressed by the master (sets it to reflect Anti-phase the first incoming Master wave pulse again).

In normal operation, Master keeps the selected data route busy at all times with Data chunks and short Gaps (Strobe periods for addressing). This prevents any of the non-addressed nodes on the route from getting a Reset - stopping them from coming back 'on-line'.

[Again, Node could generate a signal like this itself back to the Master during normal Duplex data transfer once properly addressed. This could be used to indicate a critical condition mid-way through a long data transfer. e.g. Buffer full, data error etc.]

After data transfer has been performed with the last node on the line, master uses a Reset gap to allow for a new addressing sequence to begin again.

No additional address mechanism (Serial numbers, Addresses) or software protocol are required to uniquely select and communicate with any node anywhere in the system.

Broadcast addressing mechanism

The basic inherent addressing scheme outlined above can be extended slightly to provide a useful network feature especially useful for Digital TV distribution and Videoconferencing.

Often it is desirable to send the same data to multiple nodes on the network simultaneously. (E.g. the face of the person who is talking for Video conferencing).

If the state of the pulse wave first sent to a node (Which is still should always reflect Anti-Phase) was latched, and if this state were '1' then after the strobe period, all nodes addressed with a '1' could still be enabled to receive the data on the network.

Nodes not intended to receive the broadcast data would be addressed with a '0' data pulse wave.

Eventually the Master pulses the node selection right trough to a final passive terminator then begins to send the broadcast data.

System operates in half duplex since none of the nodes addressed for broadcast try to talk back.

All nodes which were addressed with a '1' will receive and clock through the data.

Nodes must be intelligent enough to know if they are on Odd or Even so they know to invert the data.
Three level system allows for multispeed operation because overly fast data transmitted to a node with slow AC response automatically is attenuated below the receive threshold. Attenuation by cabling also prevents low speed nodes from ever seeing high speed data at the ends of the line .

DC (or low frequency AC) power distribution

Examination of the circuit diagrams shows a good DC current path right throughout the network. This path begins at the Master end and passes through the transformer windings. Current is returned through the braid of a Coax cable (or other conductor for twisted pair or Microstrip).

Internet node:- FIG13

The 'Internet' node is a simple deviation from the slave node but is especially suited for combination with Routers (described later) to form a Interconnected network (Internet) of any particular structure. Internet structures are known for their biult in redundancy

The Internet node differs from a Slave node in that it can be accessed by a higher level device (e.g. a Master device) from either port. To achieve this it incorporates three RF reflector switches instead of two and some additional logic.

When the device is in communication with a Master unit from one side, the other side is effectively 'locked out' because when in communication, the node is configured for constant reflection to the Master it is in contact with (either open or short circuit). In both these cases, the series inductance of the broadband transformer presents an AC "open circuit" condition to a Master trying to access the 'engaged' internet node from the other port no matter if the node is reflecting open circuit or closed circuit to the Master in control.

When a master moves down a line of nodes during addressing it can easily find an 'Engaged' node because the reflection of pulses are 'Open circuit' and so produce an In-phase reflection. Normally, a node always responds to the first pulse seen from the master with a 'Short circuit' reflection which results in an Anti-phase reflection.

Simultaneous access to a node is unlikely (there is a very short time period to for a node to flip over). If it happens, received quality errors by the master which looses toss will soon indicate that the line is engaged beyond it's last addressed node. As an option, a Master can retry the node until it becomes available by repeatedly sending pulses to it. Each will be reflected by an 'Open circuit' (In-Phase) response typical of an engaged node. Only when the other Master has issued a node Reset (by virtue of it's line going quiet for the Reset period) will the Node be armed for re-addressing. As soon as it is, the node will return a correct Anti-Phase return response.

Reflective Isolation of Internet Nodes

A unique property of the system is that two adjacent nodes on the same cabling can be in communication with two completely separate Masters. The two systems (which would be left and right as the diagrams are presented) do not interfere because all Master energy from both sides is reflected back towards where it came from giving reflective isolation. A large internetwork can be imagined with many masters and nodes. Reflective isolation permits simultaneous activity on multiple branches of the network (and two separate communication channels on one length of cable) without having to incorporate special measures. Total data rate can expand as the system grows.

SIGNAL ROUTING

- Implements a combination "Ring" / "Star" topology as well as Internet topology (Grid)
- Allows for much greater expansion in the number of nodes connected without exposing the data pulses to too many somewhat spuriously reflective interconnections (relative to putting all the nodes in a long line or loop).
- Makes it easier to expand networks.

Router / Terminator Operation

Referring to the diagram of the router. This is made up mainly of components and blocks already described for the Internet node. These wont be described again. Another block labelled 'logic block' will be described in words, not an electrical diagram since implementation of this logic is obvious.

In operation the Router behaves a little bit like a Node (uses same signalling) but has no need to send or receive large amounts of data. The main purpose of the router is to allow a Master to be able to quickly address specific nodes in a large system and to isolate the bulk of the nodes from being exposed to the Master output pulse waves (which they would only tend to attenuate or spuriously reflect).

The router has three ports and so allows for a single Coax bus to be split into two or allows for three coax buses to be joined depending on which way it is perceived.

The basic Router can only route a signal from one port to one other - effectively connecting them for RF signals. One port is always 'Open circuit' when looking into it. Being a three way switch allows for an easy implementation but multiway routers could be envisaged.

In keeping with the architecture mentioned for the Internet node, the Router has inherent logic to naturally signal 'engaged' by reflecting In-Phase (open circuit) to any Master pulse which arrives at the port which happens to be switched out.

The router can be controlled from any one of it's three ports.

On power-up, special RF switches initially switch in proper passive terminating resistors of the correct characteristic impedance for all lines. (Otherwise all the lines would have been Open circuit). The router never reflects back energy Anti phase so doesn't require the Short circuit to AC ground RF switches as are needed in the nodes.

The reason for this is to allow any Master whose addressing sequence pulses down to a unswitched (available) router to be able to distinguish the response of this available router from the response of a node. Nodes respond with an Short-circuit reflection for the first bit they receive (following a reset) whereas the absorption of a Master wave will give a 'non-response' which the master can identify as coming from an available switcher.

The Router is switched by the first valid Master wave pulse which it receives from any of the three ports. A '1' wave pulse flips the router to the left hand port (as viewed from where the selection pulse entered) [Clockwise]. A '0' pulse flips the router to the port to the right hand path [Anticlockwise].

Once a Router has been switched, its direction cannot be changed until a Reset condition (long line quiet condition as described for the nodes) is detected on the Port which instigated the switching. The third port becomes 'Open circuit' to act as an 'Engaged' signal to any Master node trying to change over the router from that port (same as Internet node notes).

It can be seen that all the nodes on the non-selected line of the router have no signal and this will soon be interpreted as the 'Reset' condition which primes them ready for a later addressing. *(This 'Reset' condition wouldn't apply to nodes on that route which are being communicated with from the other direction by an active Master [see notes on Reflective isolation principle].)*

After a Reset period is detected from the port which set the path of the router, all the inputs are returned to the Characteristic termination resistance (absorb, i.e. non reflect) and the router is available for control by the first Master pulse to arrive on one of the three ports.

Termination feature
Another feature to build into the Router logic would allow for the use of the Router to make the Characteristic impedance termination persist for a particular port to furnish a convenient termination when using the Broadcast feature (Broadcast feature requires that no multiply addressed nodes reflect anything which means the end of the line must be a Characteristic Impedance termination).
- The previous method of router direction selection can be supplemented with logic which detects when the Master sends a routing direction pulse wave is followed by a strobe. Normally the Master wouldn't do this because a router doesn't need a strobe pulse - usually, the master generates the pulse for the first node on the switched-to port immediately following the route selection pulse.
- The unique sequence is easy to generate and when decoded it lets the router hold the Characteristic termination impedance for the input port. The router ignores the route selection just specified. Logic can be present to still allow for the other two ports to be switched together by a master operating on either one of those ports. The 'engaged' signal would only be returned should an attempt be made to route onto the port which has the persistent Characteristic termination.
- Reset condition detected from the characteristically terminated port can clear all the engaged logic and return port to normal operation.

DC power (or low frequency AC) can be conveniently added to the network at the Router junctions to maintain a good low resistance supply of power to the nodes and computers attached.

[FIG 15] The routers can facilitate large interconnected arrays of nodes, facilitating redundancy in the possible paths between nodes. Addressing paths can 'snake' around the network. When a path is found to be inoperable or engaged, an alternative addressing path could be tried (or could wait for end of engagement). The topology directly implements the 'Internet' architecture arrangement without any complex or expensive electronics or software and can let the internet be brought right down to the level of small actuators or sensors.

At very high data rates (e.g. Microwaves) use could be made of PIN diodes incorporated into the hollow metal wavegiudes of an microwave Circulator arrangement to facilitate routing.

Self Determination of Network topology

- A master controller can fully investigate and establish the topology of any network onto which it is attached by a self exploration process.
- After issuing a node reset condition (extended length gap), Master moves through all the nodes on the highest level line using addressing method (Pulse and Strobe method) as described before.
- Master sends out binary '1' waves followed by strobe periods. This can happen as a continuous stream. The reflected signals from each node should be "Anti-Phase" waves if they were addressed properly. Engaged internet nodes reflect 'In-Phase' and can be retried until free as outlined above.
- When a wave reaches a router switch, the state of the Wave determines which direction the router will switch. If the router has already been switched by another master, it too will return an Open-Circuit 'Anti-Phase' pulse as an engaged signal. Otherwise, to identify itself as a Router rather than a node it absorb the wave with a resistance equal to characteristic wave impedance to produce the No-reflect signal (third gap state when it reaches Master) before switching to the direction specified in the state of the Wave which was absorbed to route further signals down that path.
- Master later sees the No-reflect (Gap) pulse in it's input stream and so knows there was a router and knows which way it told it to switch.
- Ultimately the master reaches the end of the "All '1's" path through the network. The end of a particular path is a final passive terminator of characteristic impedance. Master knows it has reach the end of the line by having all it's output waves absorbed and so receives a constant Gap condition.
- Master now knows many nodes are on each part of this particular 'All 1's' route through the network, the location of the routers and the end of the path,
- Network investigation continues by the Master re-running initially the same sequence but upon reaching the last router in the system, it sends a '0' wave instead of a '1' to investigate the branches off the last leg of the previous route.
- Master iterates until it has fully explored every branch and chain of the network to build up an internal network map of nodes, routers and terminations.

- For Internet arrangements (Multiple Masters), investigation of a route might lead one Master to Find another on the route (assuming the other Master is Quiet). Intelligent Masters can have software protocol so they recognise each other and share information. This could be the basis for a parallel processing system.

PARALLEL PROCESSING SUPERCOMPUTER ARCHITECTURE

Especially when large Wide Busses (Multi bit systems) where say 32 (or more) parallel channels of the system are used (e.g. on Microstrip Media) the nodes could actually be wide Peripherals or just Silicon Memory.

Conventional Data Bus topologies (e.g. PCI bus, VME bus, NuBus) only allow one bus owner to control the bus at any one time. Total bus bandwidth is fixed and does not grow as more peripherals (Wide nodes using new terminology) are added. The proposed system of reflective Isolation between adjacent sections of bus combined with 'engaged' signalling lets every section of a bus be split and operated point to point at the full data rate. Cards which interchange large amounts of data with each other can be located adjacent in the bus. A single 'Master' program is still able to communicate with the cards individually if periodic 'idle' slots are inserted.

Standard computer Bus topologies are unable to extend more than a couple of feet in length due to transmission line and reflection effects. The invention here has no such limitations.

Signal Routers can be extended to 'n' bits also

SYSTEM WITH REFLECTION ELIMINATION (1/2 Duplex)
- Useful mode of operation for fetching large amounts of data from a distant source at high speed.
- Rejects all spurious reflections from cable.
- SEE LATER

DEVICE FABRICATION
- Suits GaAs technology (ultra high speed), ECL process technology (very speed) BiCMOS (High speed) CMOS (moderate speed).

HIGH SPEED VERSION WITH GaAs OPTO-ELECTRONICS FIG11
- The NPN reflective switch would be good to about 500Mhz using conventional silicon technology.
- PIN diodes are an alternative RF switch used into the microwave frequencies. Unfortunately, electrically controlled PIN diodes would inject large signals into the coax bus when they were turned on or off. Therefore would propose to
- could use Gallium Arsenide MMIC (monolithic microwave IC) and fabricate the switches as optically driven PIN diodes using a integrated laser on the substrate (GaAs devices allow integration of Optoelectronic components and electronic components on same monolithic device).
- with on/off times of 0.1nS, system could operate at >1Gbps.

Might be possible to make an all optical system on fibre optic based on Kerr Cell.

TDR (Time Domain Reflectrometry)
- The invention uses and detects pulse reflections on the cable as part of the signalling process
- The receiver circuitry at the Master end can be supplemented with a high resolution timer running from the 3x clock generator plus an adjustable (DAC controlled) receive threshold settings. This would form the basis of a Time Domain Reflectrometry system where the exact round-trip pulse echo time and amplitude can be monitored from Master back to master again.
- With programmable receive thresholds the Master could lower the thresholds and detect low-level reflections from cables, connector damage etc. This facilitates exact location of a fault in a line since any deviation from nominal impedance (higher or lower impedance) caused by a short circuit

or an open circuit results in a reflection. Also, when a coax cable is crushed or stretched badly it experiences a measurable change of characteristic impedance and therefore gives reflections.

PLUG-AND-PLAY.
- Master computer can easily detect the presence of the new node the next time a full newtork explore is performed.
- If TDR is incorporated then a new node can be detected and it's position (in electrical length units) can be determined by the time of flight of the first output pulse following addressing.
- A router can be added at any point to expand the system
- Multiway routers with internal terminations could be used to allow for e.g. a 8 port "extension socket" type cable into which devices can be plugged.

"WIDE" SYSTEMS
- So far the notes have concerned mainly a single bit wide channel. The system is also able to operate as a multi-bit (e.g. 16 bit, 32 bit) bus system perhaps using Microstrip line internally to a computer and twisted pair ribbon cables for external connections. It is feasible to combine 32 bit, 16 bit, 8 bit and 1 bit routes together. By starting with a 32 bit wide system, each bit could ultimately be the source of a new, independent single-bit route but could first reduce to two 16 bit busses then four 8 bit busses.

The internal data bus of a PC would 'come out' of the chassis and become the office network without intervening buffers etc.

At 300Mbps, a 32 bit system could achieve a throughput of 1.2 Giga bytes per second over a reasonable distance with low radio frequency interference (RFI / EMI).

TRANSMISSION LINE (typ COAX) MEMORY DEVICE --- simple reflection rejection system - SEE FIG16, FIG17
When attempting to read back data from distant nodes at high speeds, a full duplex operation is not practical. The problem arises from the fact that spurious reflections from the Master output pulses by in-between nodes and cable + connector mismatches gives a return signal in which the reflected signalling energy from the node can be swamped by the spurious reflections. One remedy would be to reduce the data rate (reflections reduce with operating frequency esp. stray capacitance reflections) another fix would be to have the nodes able to generate their own wave-shaped three level outputs and include a local clock generator (variable frequency to suit cabling) on every node so clock pulses by the Master were not present during reading of data from the node -- this is undesirable from the aspect of cost, complexity and power consumption and the inevitable protocol overhead probably requiring local software.
The remedy proposed here simply and fully eliminates this problem and keeps the nodes as simple as possible.

- Example of a 200Mbps system using 3x 1.66nS periods.
- Use sub-divisions of this operating frequency down to 1/16 the operating frequency or 12.5Mbps.

- Reflection data is extracted with a differential amplifier as per telephone. (Hybrid equivalent
- This signal includes all the rogue reflections of the output clock signal as occur from coax imperfections, connector VSWR, node stray capacitance etc.
- Output of the differential amplifier then feeds the Coax memory, which for 0.8x light speed coax is 10meters long and shorted at the other end.
- 20 meter round trip, shorted end forces any regular waveform put into the end of it a multiple of 12.5Mhz to be reflected and nulled at the entry to the coax line.
- 12.5Mhz has a total of one waveshape in the coax, 25Mhz has two full waveforms etc., 200Mhz has 16 full waveforms in the cable
- The coax input node is zero volts for any arbitrary regular waveform at 12.5Mhz and multiples thereof. **Also rejects non-perfect CMRR of the receive amplifier.**
- Operating frequency could be voltage controlled set by the actual response of the Coax memory line (Self tuning):- The RMS voltage (rectified power monitor) of the receive signal can be a digitised variable known to the Master controller. Only when the frequency is exactly right do get 100% cancellation of input waveform. **Can periodically route the Master output waveform directly into the coax memory for a tune-in period** Frequency can then be adjusted using a DAC driving a varicap oscillator until get the minimum reflected power measured at the coax entry -- system self tunes to suit the coax memory
- Coax should be low loss type. Any return loss in the coax will leave residual signal on the node. Cheap coax (£0.50p /m Satellite TV 8mm dia) has about 2dB round trip attenuation @400Mhz. (which is the fundamental for 4 segment signal). This is about 20% (i.e. it will attenuate the highest F reflections by 5:1, much better for lower F reflections).

- Could be replaced with a solid state CCD analogue memory, but in network applications, an extra 1m to 10m of cable (depending on minimum data rate) would not be noticed amongst several hundred meters of cable.

- Good substitute for Coax in this memory application is Microstrip transmission line with capacitive stub branches to slow down the effective velocity. -- this would be especially useful in PCB backplane applications.

Mode of operation:-
- With example of 10m of 80% speed-of-light cable, there is a 20m round trip time. Voltage waveforms travel down the coax and travel back, inverted in voltage but same magnitude towards the transmitting end.
- Considering the example of the leading +Ve edge of a regular square waveform, it will travel down and return as a pulse of opposite polarity in transit time (round trip time) of 80nS. For a repetitive waveshape of period 80nS, the next rising edge appearing on the output of the coax drive amplifier corresponds exactly to the time when the previous +Ve edge reappears as a -Ve edge at the entrance to the coax (having been reflected right down the coax and back). The input and reflected voltages cancel because the series drive resistance into the coax matches the wave impedance of the reflected wave (assume output impedance of transistor is zero). This cancellation persists for the entire time of the +Ve period of the square wave. Similarly, when the -Ve portion of the driving square wave presents itself to the series resistor, there will be the reflected (and so +Ve) waveform of the earlier pulse. Again, cancellation occurs. Cancellation applies to any arbitrary waveform which is repetitive within a time period integer divisible with no remainder into the round-trip time in the coax.
- When fetching data from a Node, master has to work in half duplex mode. It still sends output pulses to clock the remote node but these pulses are of constant binary wave values (either a

constant stream of '1' waves or '0' waves). These pulses are therefore repetitive within the round trip time of the coax memory and so reflections from these output pulses however caused and wherever generated on the Network routes are cancelled no matter what the phase relationships of the individual sources of spurious reflection and how these waves combine.

[Assuming the master has primed the Network cable with sufficient clock pulses that the energy has propagated the full path and spurious reflections pattern is fully established and detected and the coax memory is primed and is cancelling this received waveform], the Node begins to output data in the Previously described manner of Short Circuit or Open Circuit reflections.
- This energy propagates back to the Master receiver and on to the Coax memory drive amplifier. Initially the coax memory produces cancelling or additive effect this desired signal since what is streaming back out of the coax memory entry point is the energy which is cancelling only the repetitive unwanted signal. A very clean reproduction of the desired signal is produced with the repetitive rubbish removed. This first pulse goes through to the three-level detection circuit and Pulse quality checker to make a normal data pulse reception as per normal.
- What happens to the next pulses is different to processing without the coax memory because the first pulse has now been entered into the coax and will at some time reappear back again reflected and inverted.
- Imagine that the coax memory has a round-trip storage time of 16 data pulse cycles (e.g. running at maximum speed) then 16 pulses can enter the coax line before any effect is seen at the entrance of the coax from the first pulse. The first 16 pulses are therefore recovered correctly by the normal logic.
- Subsequently the 17th pulse becomes added to the reflected inverted version of the 1st pulse which now appears out of the coax memory at the time when the 17th pulse is coming in. Because the coax round-trip time is an exact multiple of the pulse periods, the waveforms are added in-sync. The diagrams show the results of cancellation. [FIG
- All three possible final states are detected by the level detection logic. Also since the 1st pulse was received normally (addition-free) then digital logic can determine what the 17th pulse state must have actually been to produce the end result state picked up at the 17th bit time. By always maintaining a digital record of the previous 16 states, the true state data can be established for each pulse as it comes in so producing a normal, proper binary bit stream for the Master.
- Half duplex fetching operation alternating with broadcast transmission allows for Video confrencing where one frame of video data can be gathered then sent to many different locations on the network.

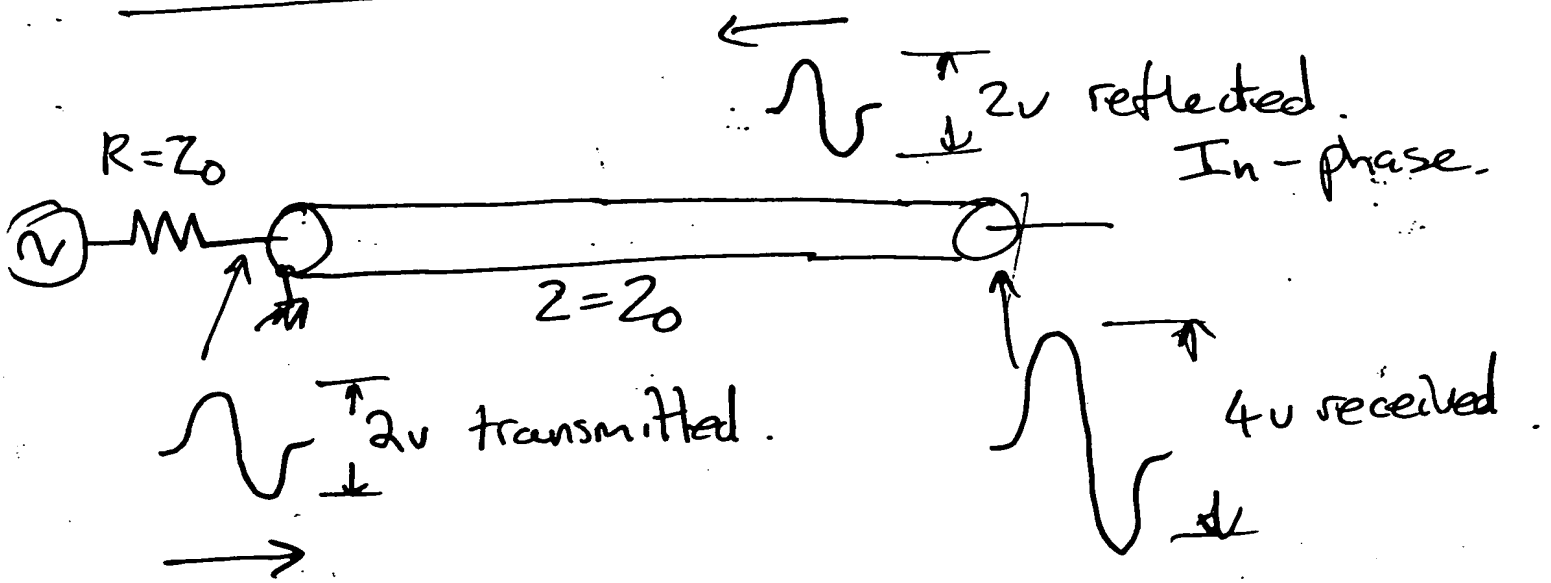
DIGITAL MEMORY COMPENSATION + ADC

- With TDR included, system can know the distance (in terms of electrical length) to all nodes. It is possible, after determining the spurious response of all nodes at all frequencies together with the electrical length information (phase information) to digitally predict what the spurious reflection pattern would be to any set of output data produced by the master controller.
Using a very high speed ADC convertor to receive the reflection signals, the predicted reflection pattern can be subtracted (in software) from the actual (contaminated) return signal codes leaving only the reflection response from the node to communicate with.
An alternative would be to use a high speed DAC and use it's output to subtract (using analogue summer amplifier) from the received signal to leave the desired signal.
This system would be very difficult to implement in current technology but could in the future allow for full duplex communication with remote nodes at high speeds on existing cabling.

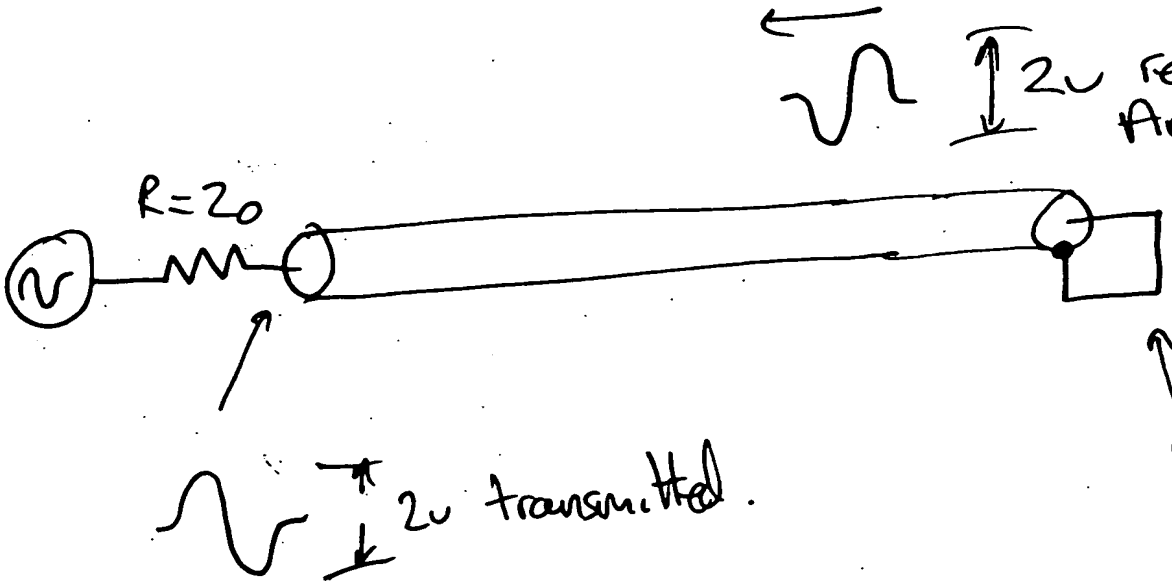
Transmission Line Phenomenon.

FIG 1

Open Circuit termination



Short Circuit Termination.



Signalling levels — Clock and Data Encoding.

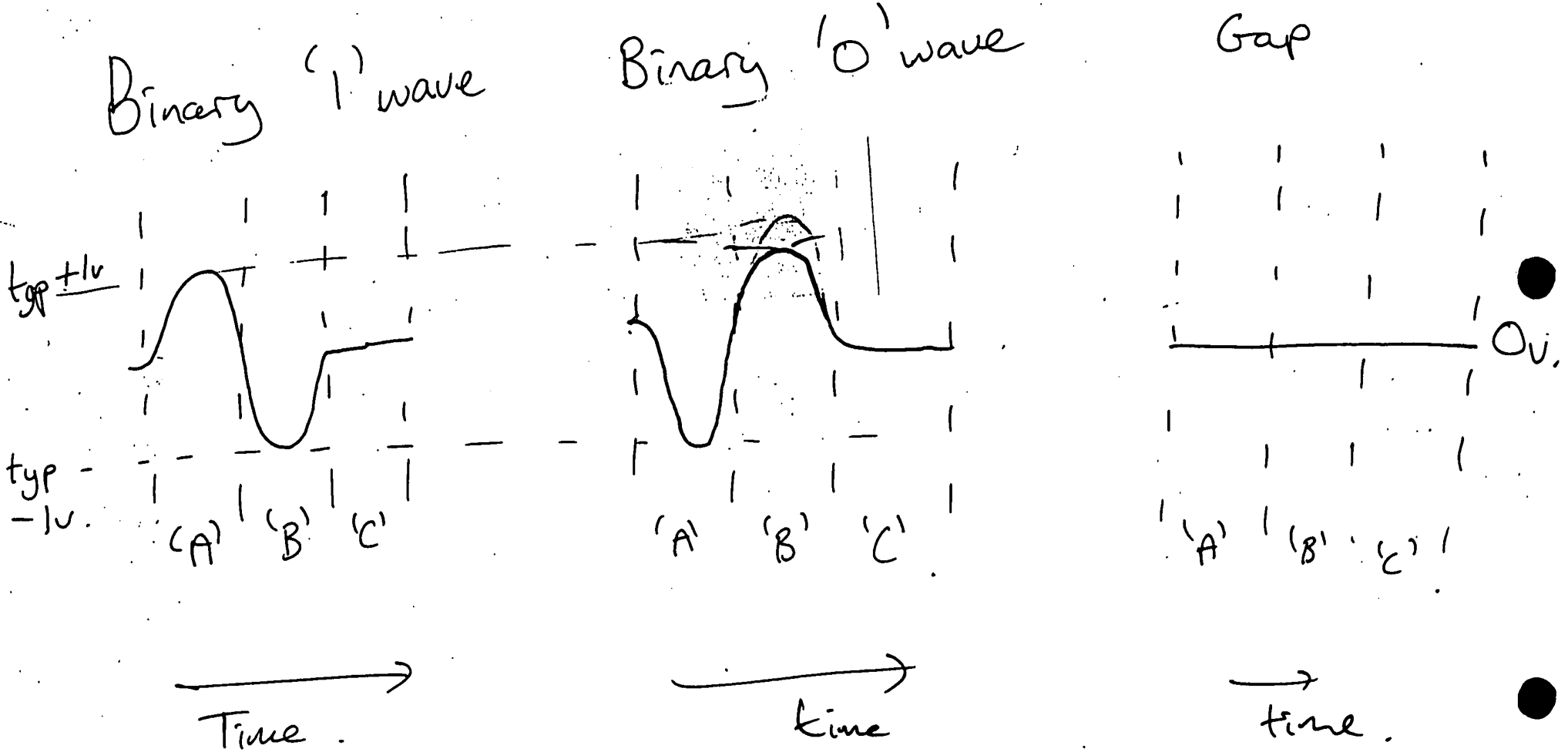


Fig 2

Master End Electronics. — block diagram.

Fig 3

MASTER UNIT

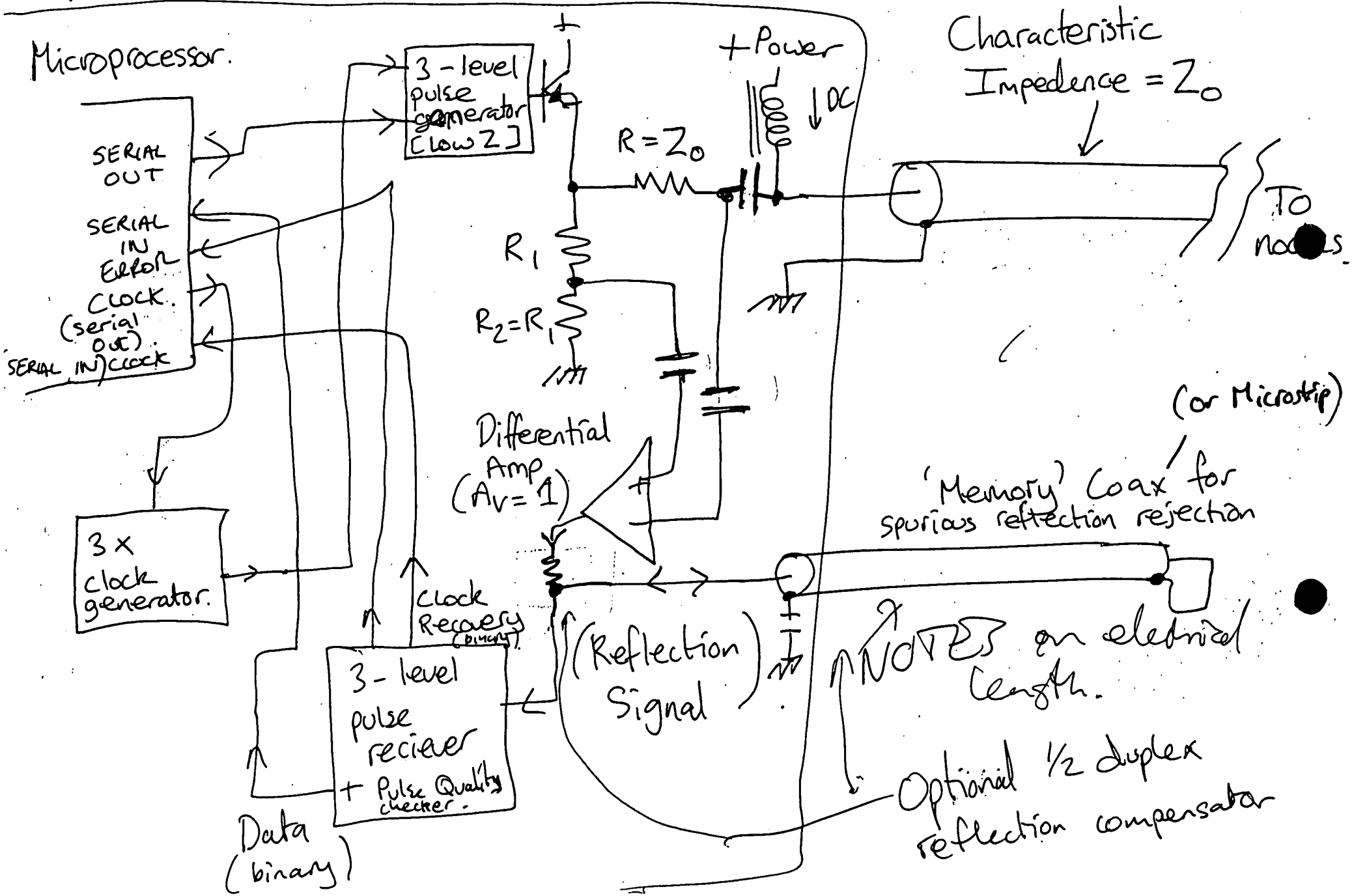
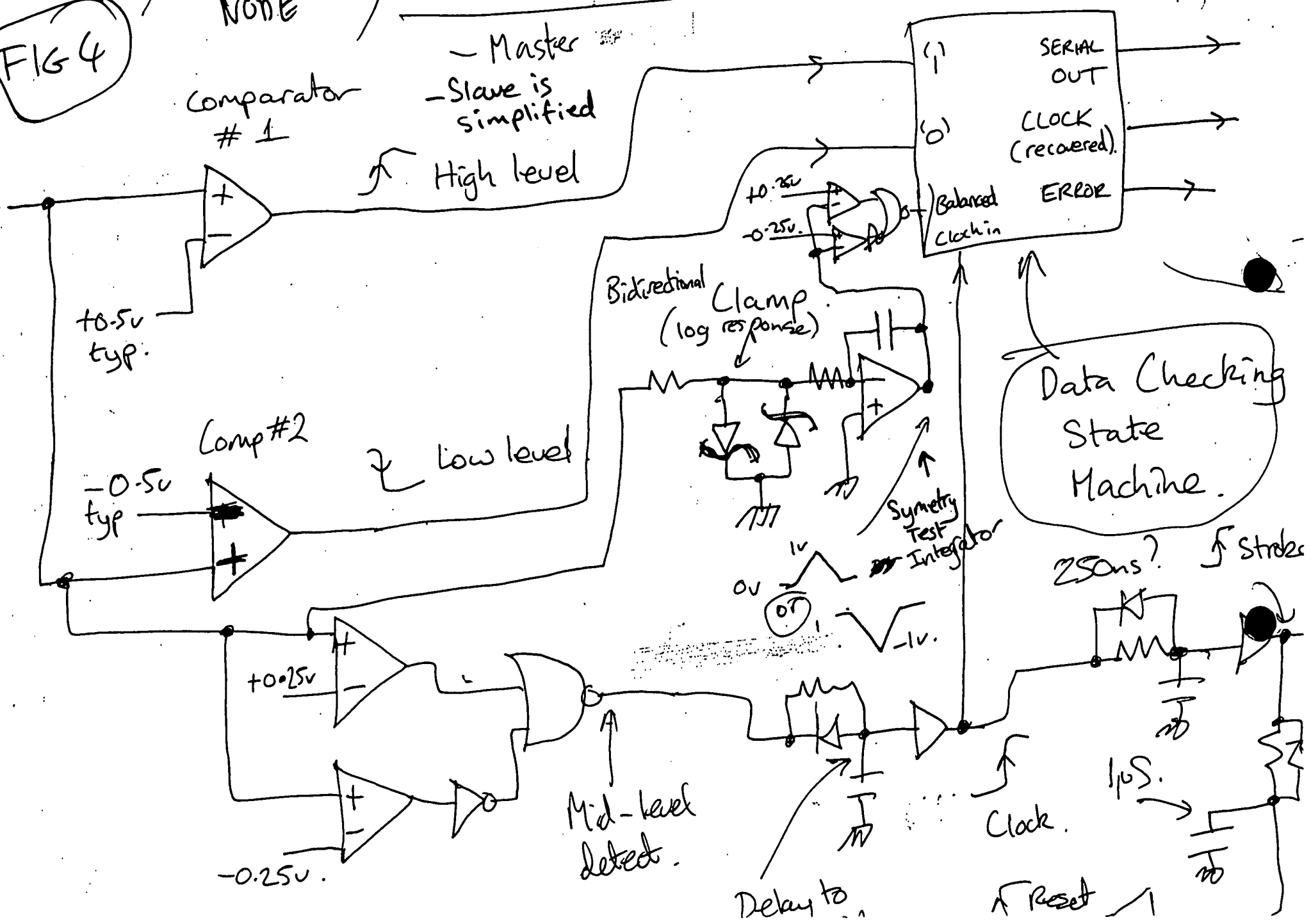


FIG 4

(MASTER & SLAVE NODE)

3-level pulse reciever + Quality checker.

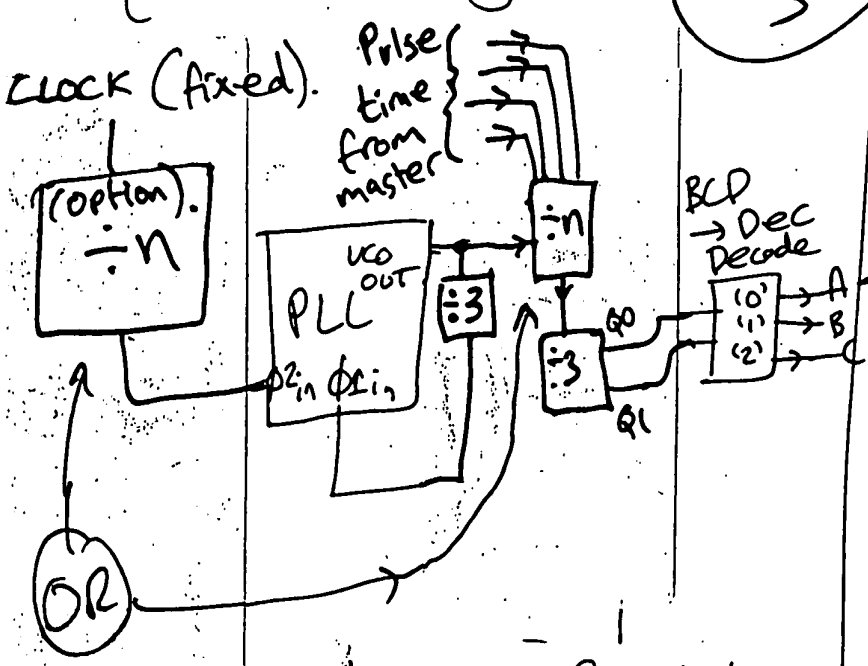
- Master
- Slave is simplified

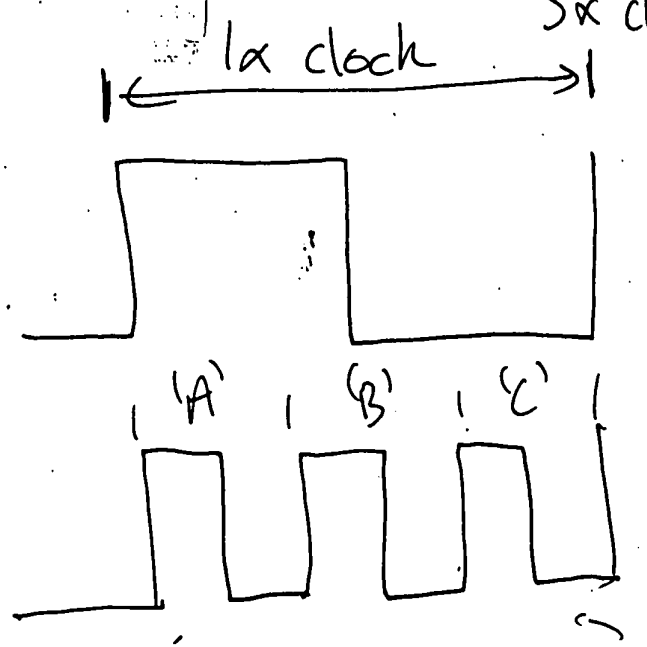


(MASTER)

3x clock generator. (Master Only).

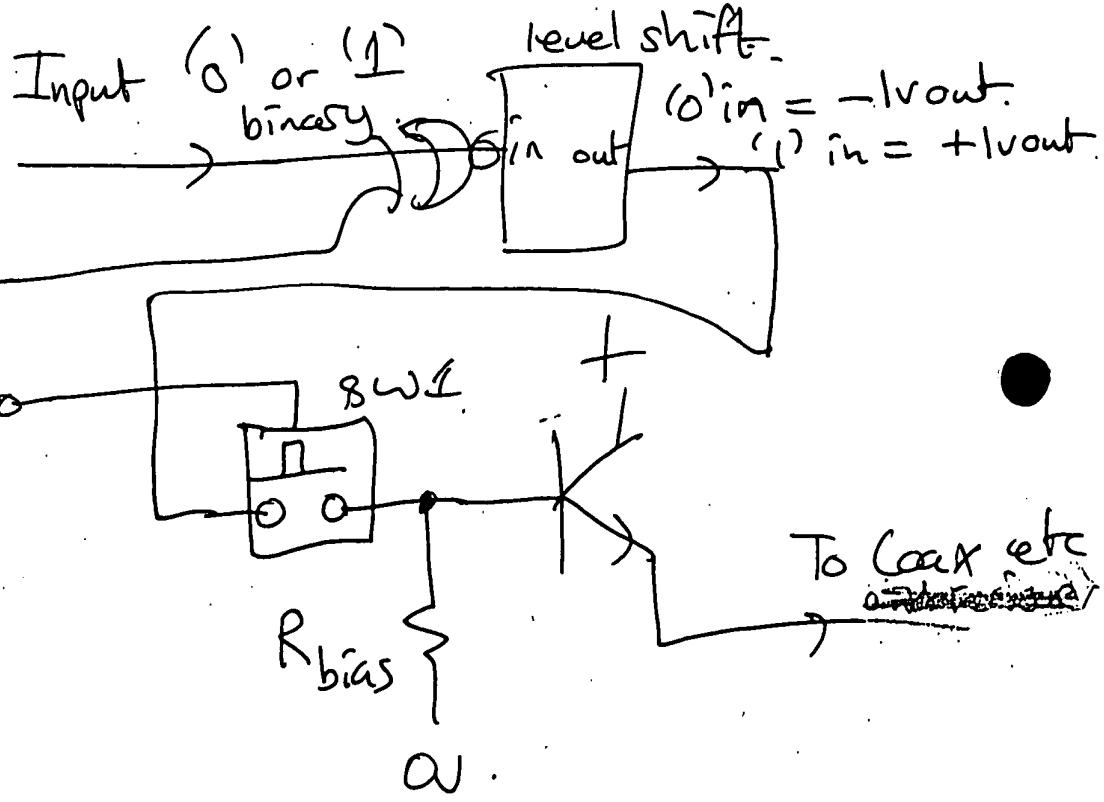
FIG 5





(MASTER)

3-level pulse generator. (Master Only)



Notice

On 'C' active, SW 1 turns off so output goes to 0v by virtue of R bias.

Node Electronics (Basic form)

Fig 6'

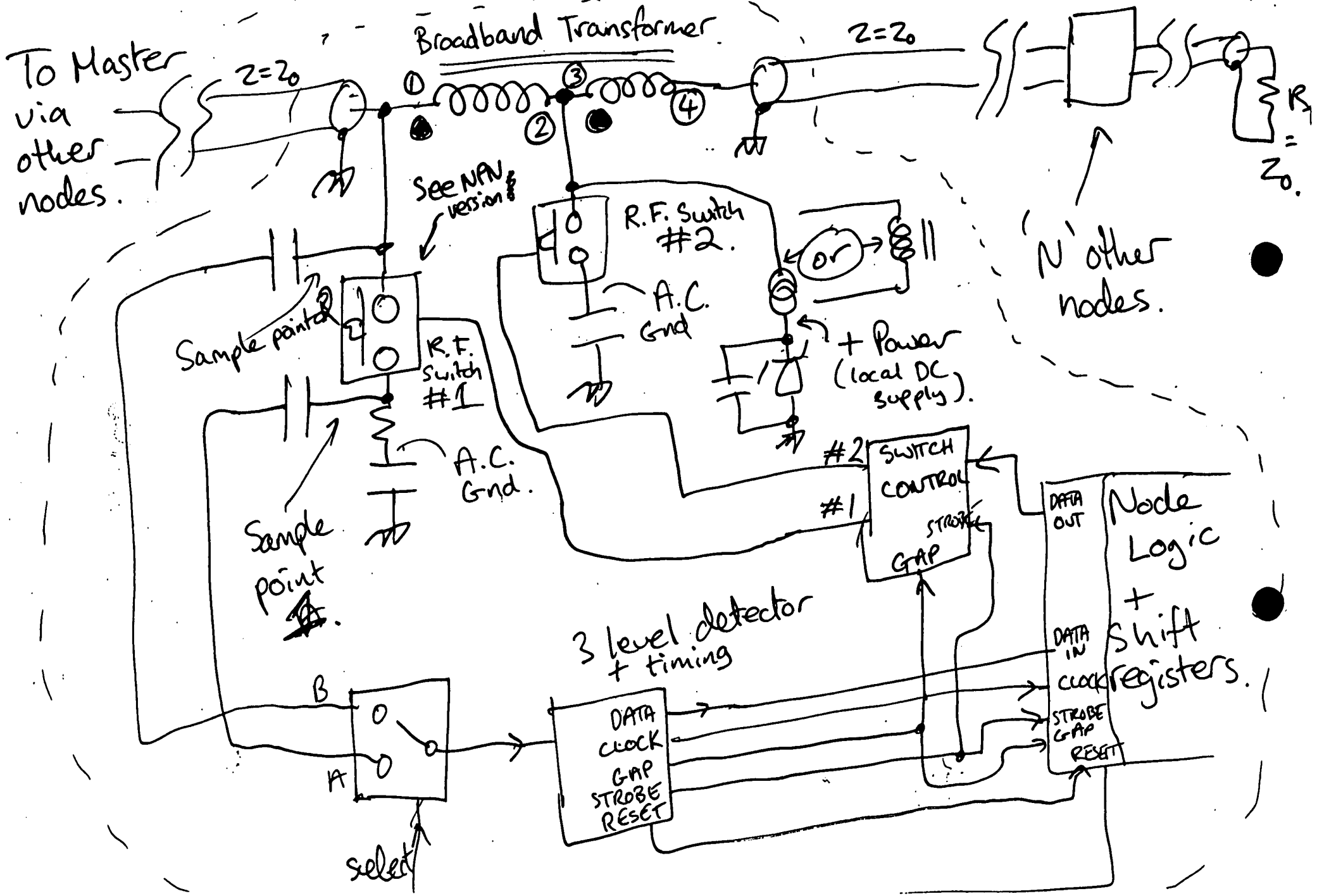


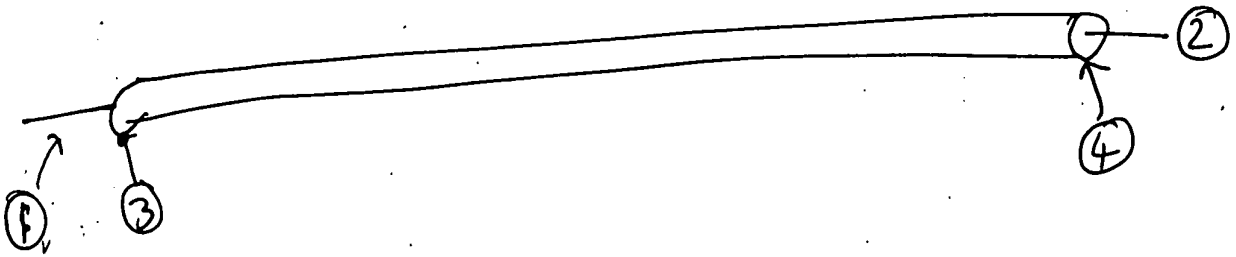
FIG 7

Broadband Transformer

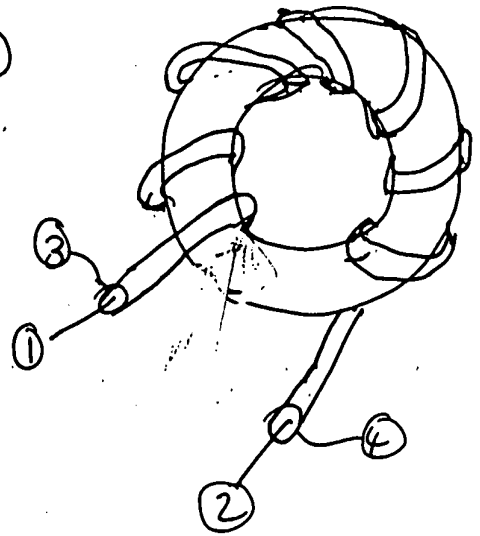
– Standard 1:1 inverting transmission line design.

Coax Option

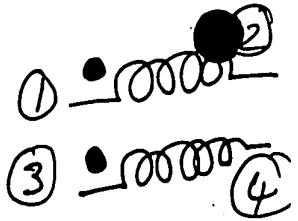
Coax prior to winding.



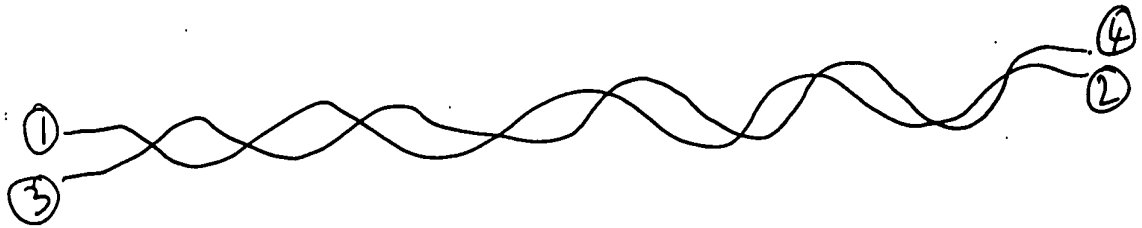
Complete Transformer

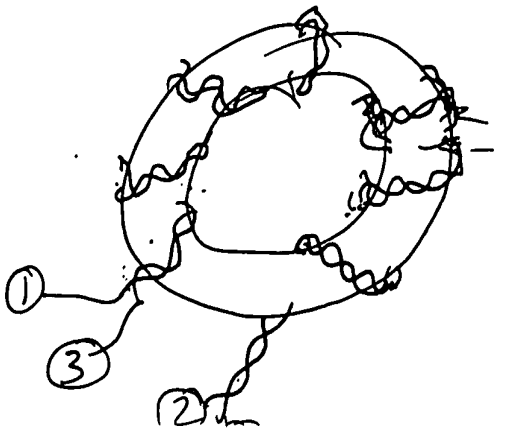


Circuit diagram



Twisted Pair Option



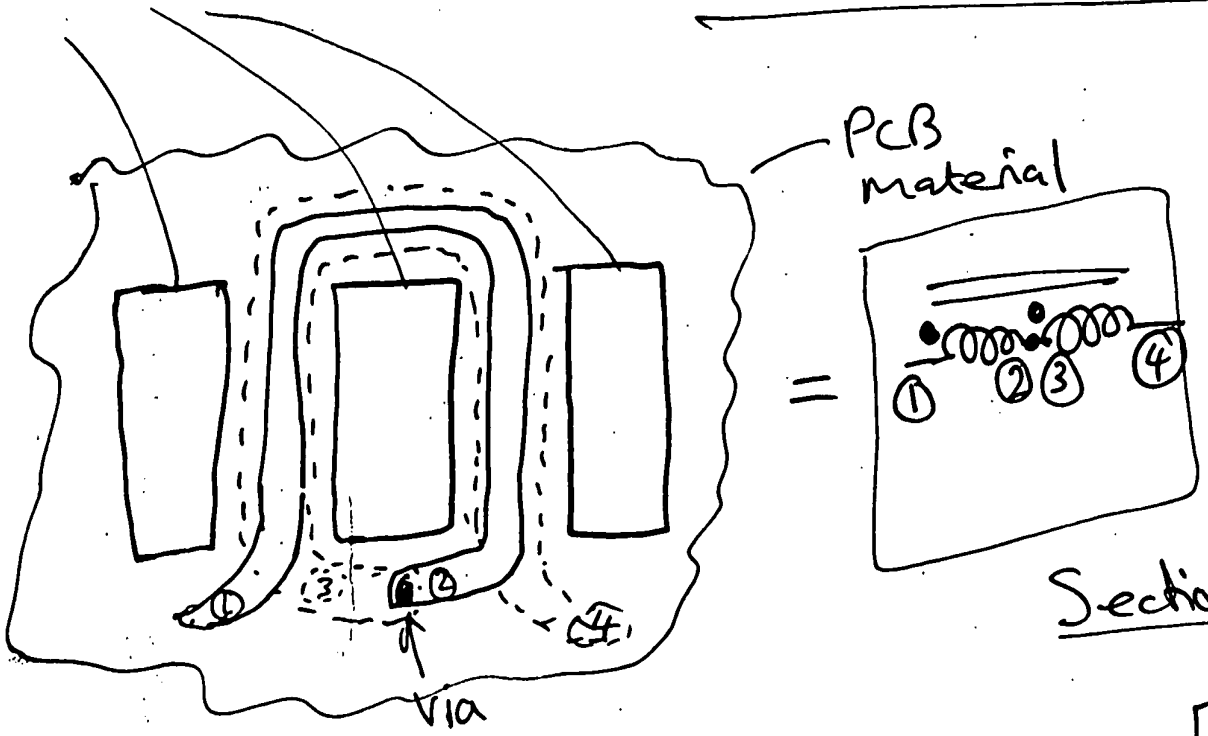


Microstrip / Planar → See separate diagram.

FIG 8

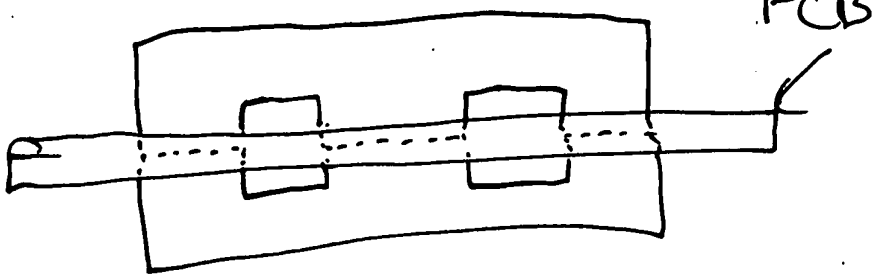
Microstrip Planar Transmission line transformer

P.C.B. Cutouts.



Notes
- Single turn shown.
  - could be multiturn.
- Standard planar PCB magnetics used
- Can integrate other electronics on PCB

Section view of finished unit.

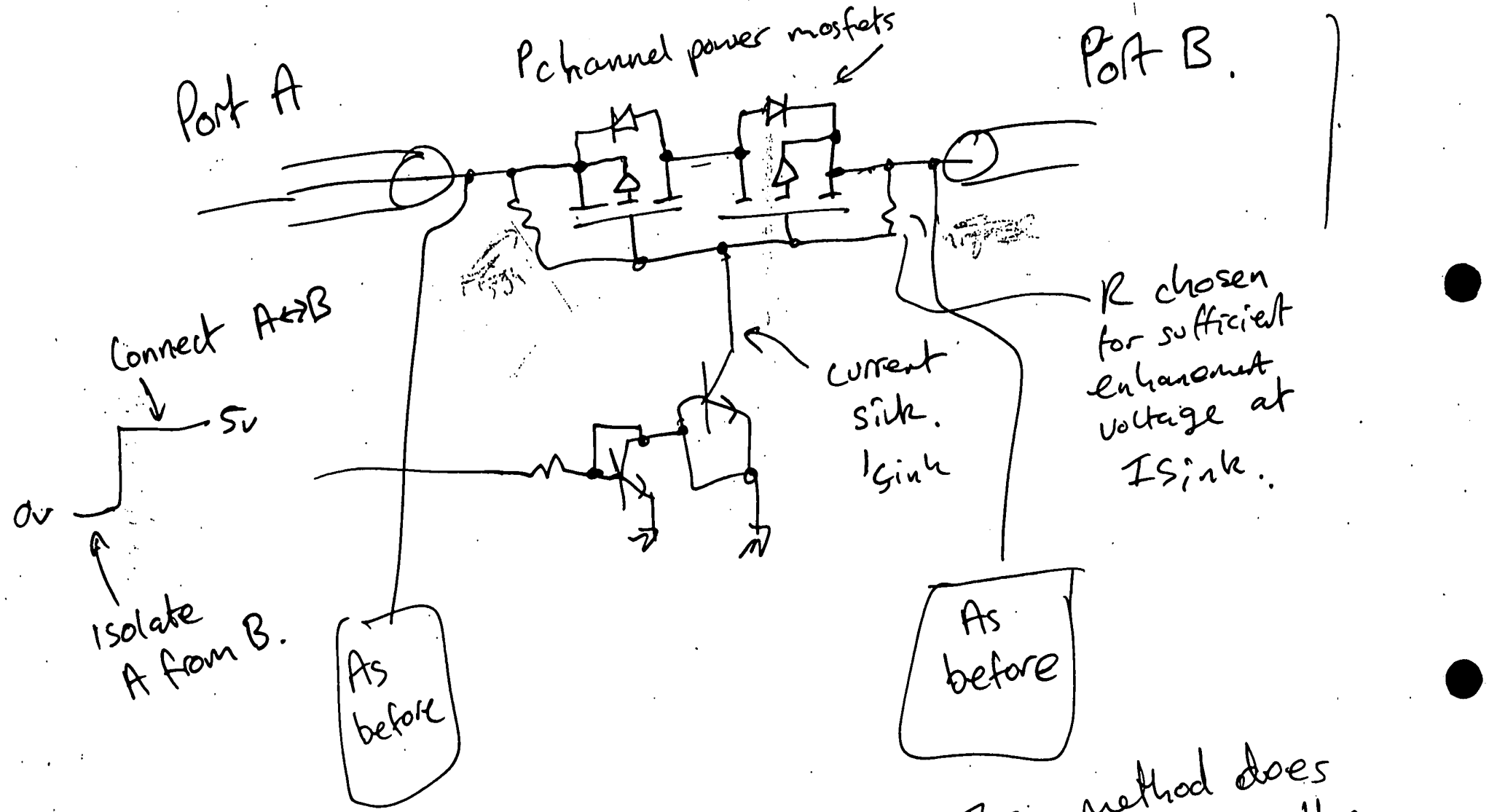


Side view of one 'E' core (planar magnetics).

Two core halves clamped together.

FIG 9

Alternative Node Arrangements (All electronic transformer substitute)



Notes: ① This method does not invert the through-signals.

voltage would allow use

Preferred RF reflector / Signal pickup point.

FIG 10.

(Node only) — Bipolar Transistor Version.

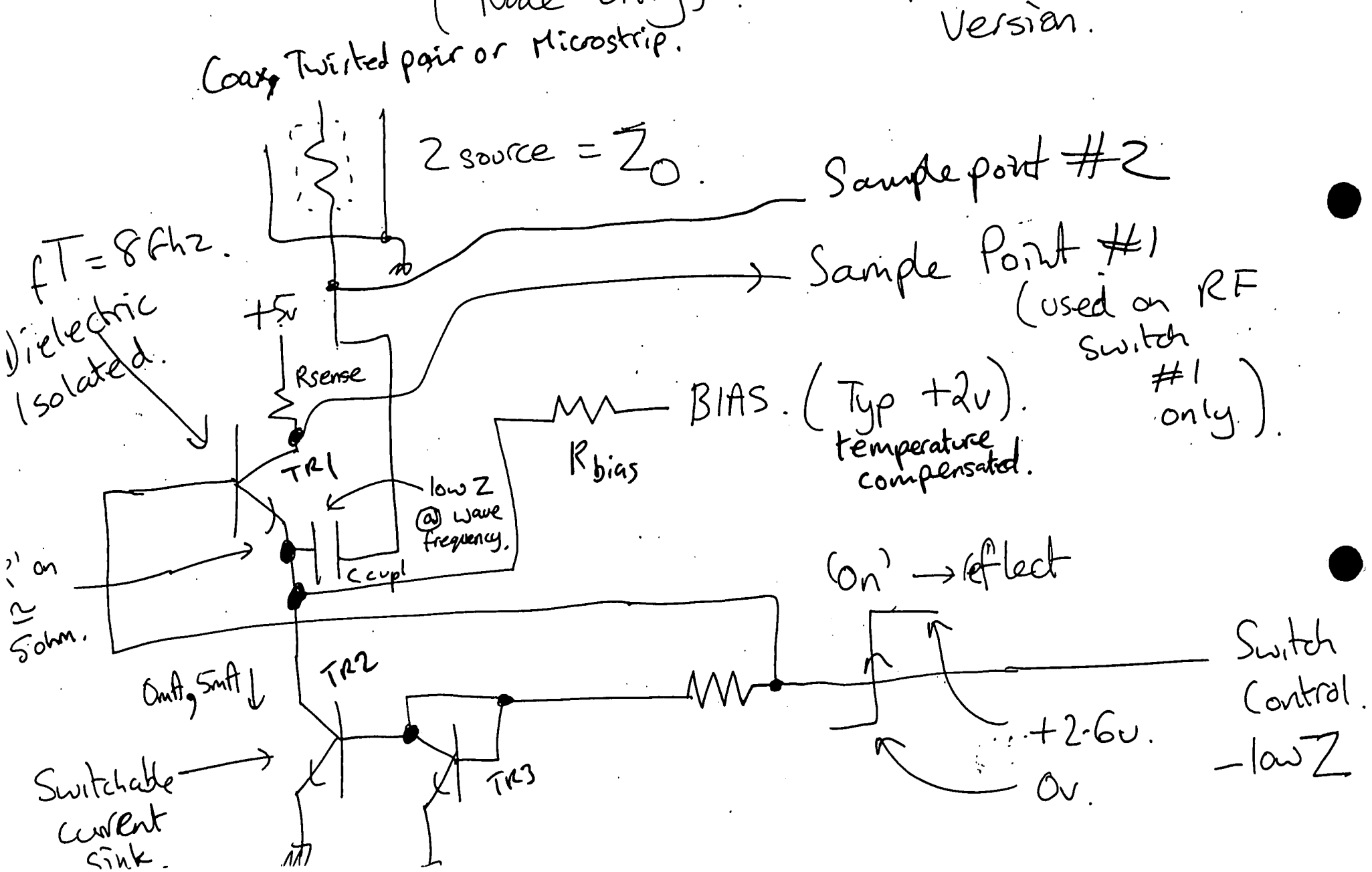
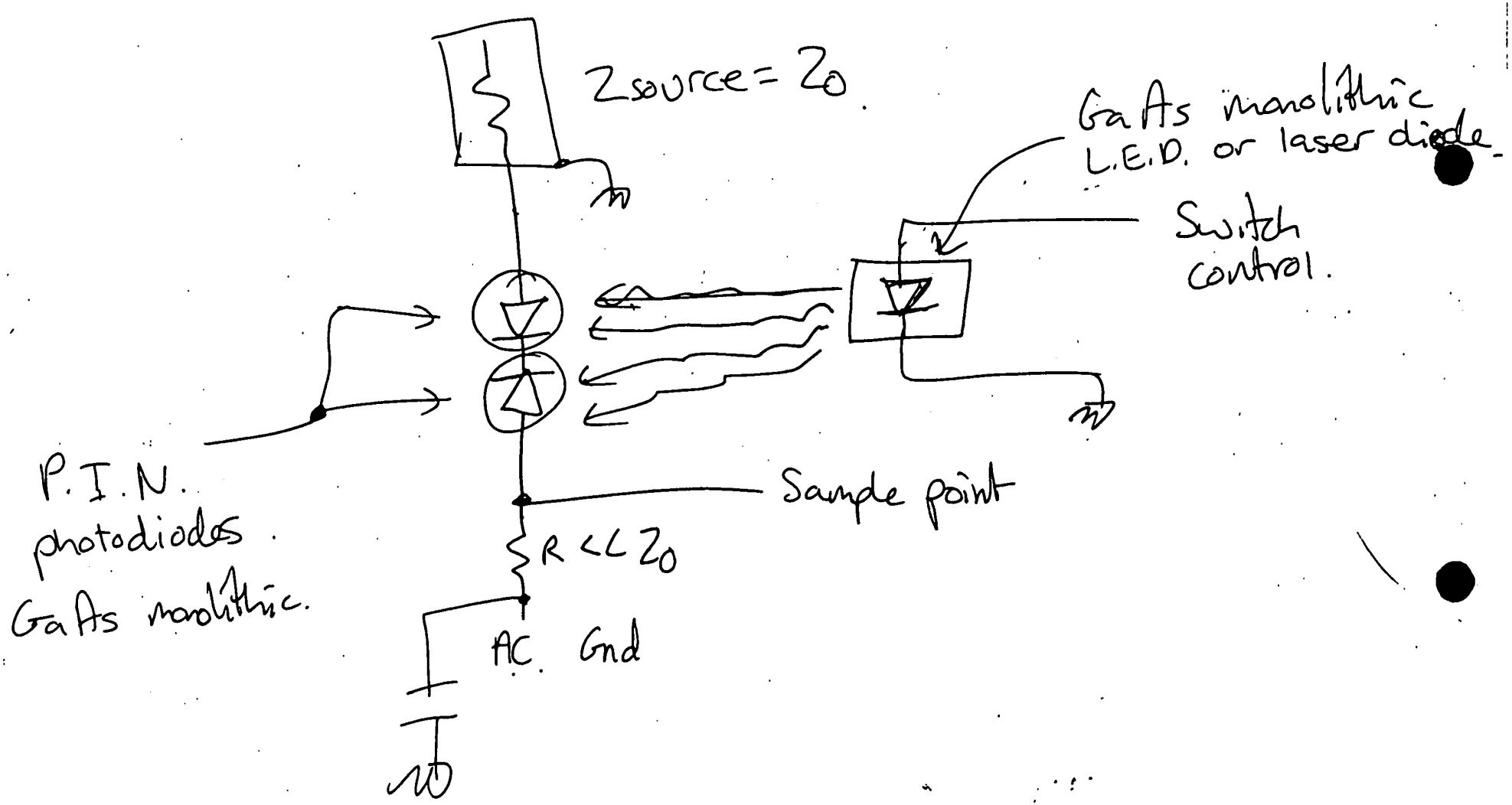


Fig 11

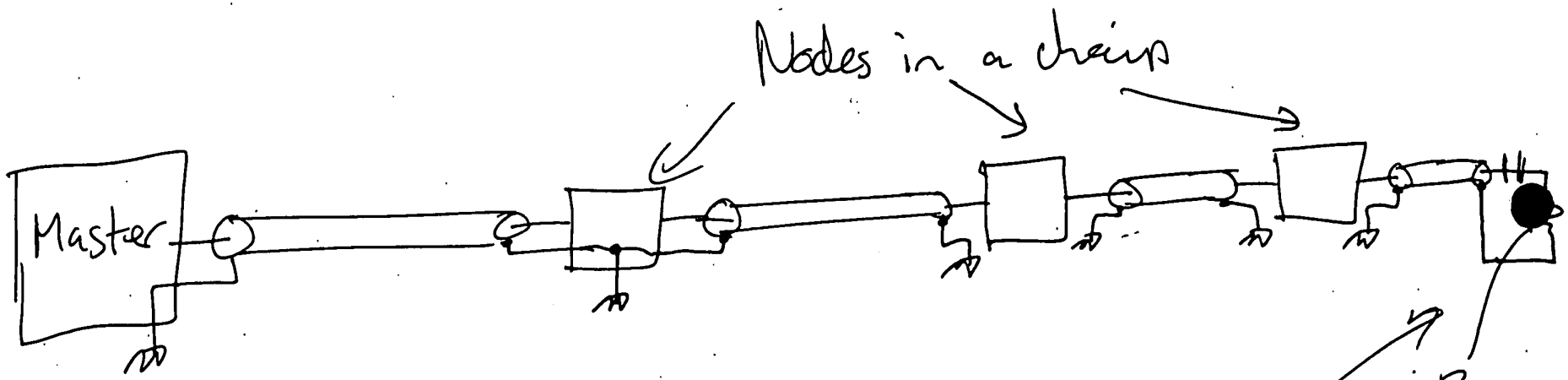
R.F. reflector (Node only)

Possible GaAs Photo electric version.



Simple Master / Slave System

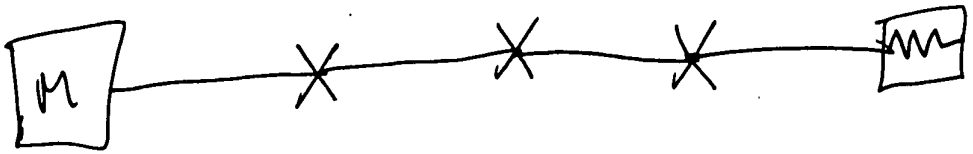
FIG 12



Schematic form

X = node

= Passive Termination



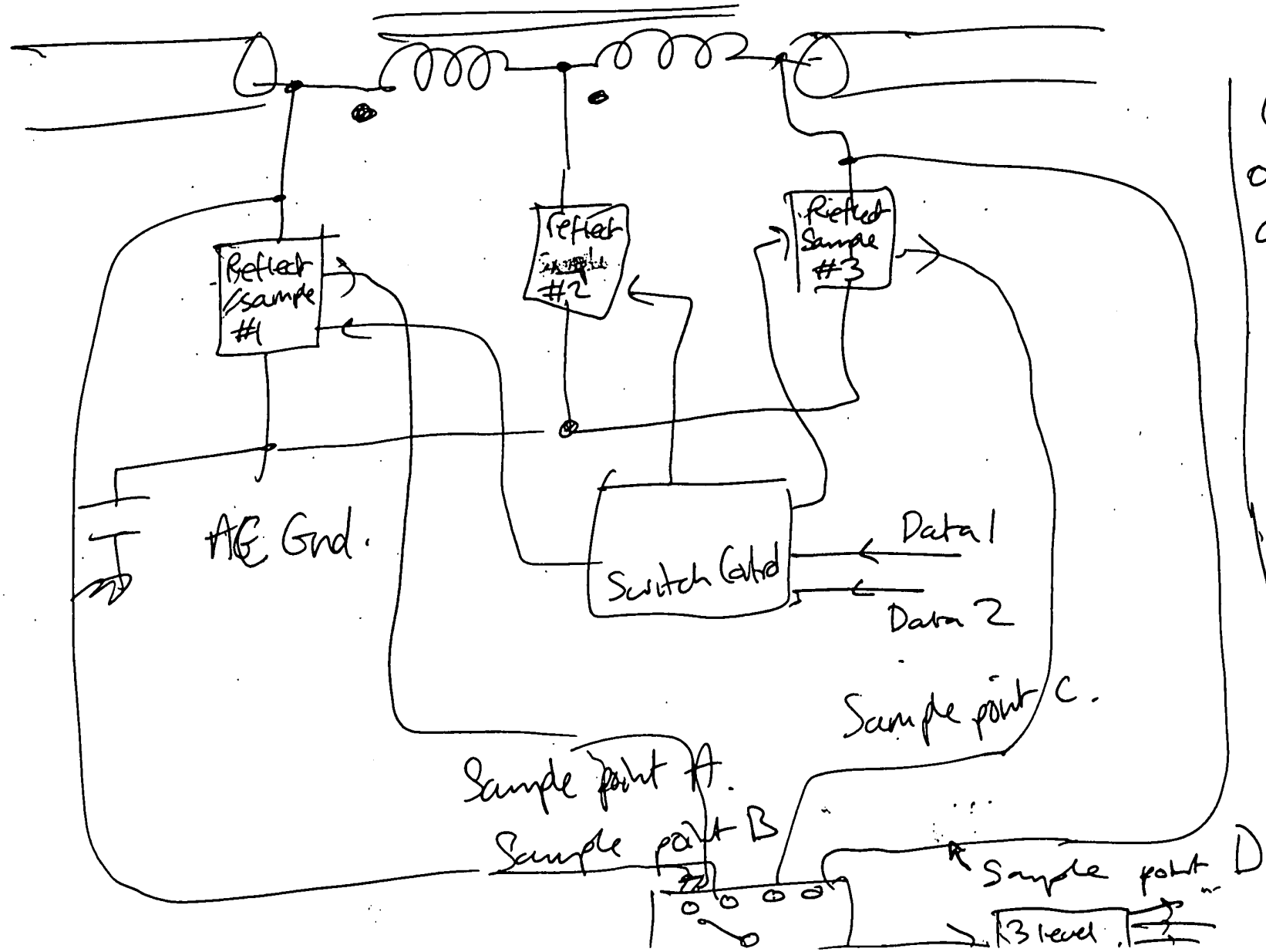
Passive (absorptive) terminator.

FIG 13

Internet Version of Node → ADDITIONAL FEATURES ONLY.

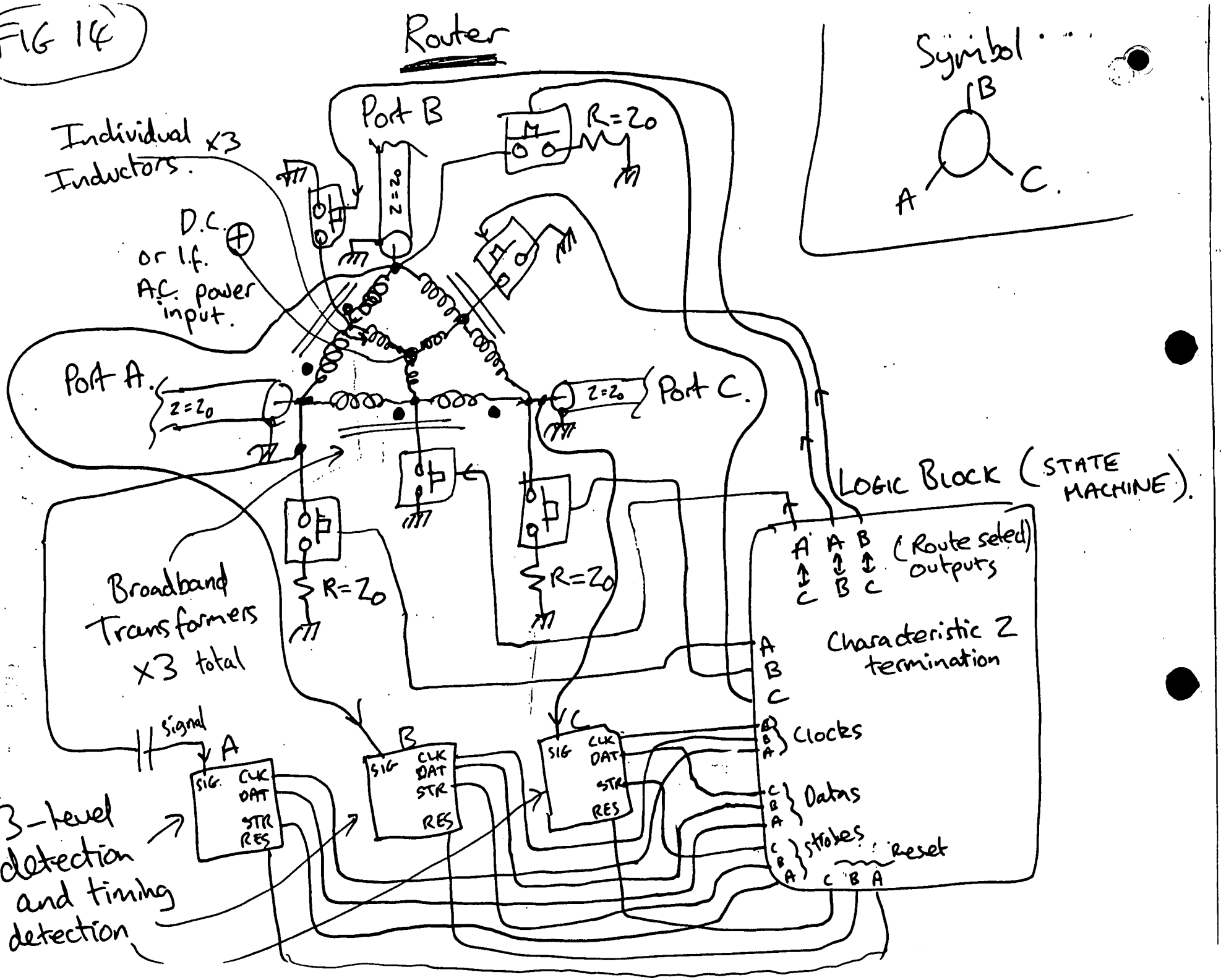
Nodes and Masters
Routers ←

Nodes and Routers. → Masters

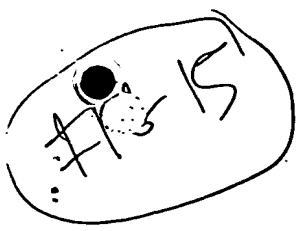


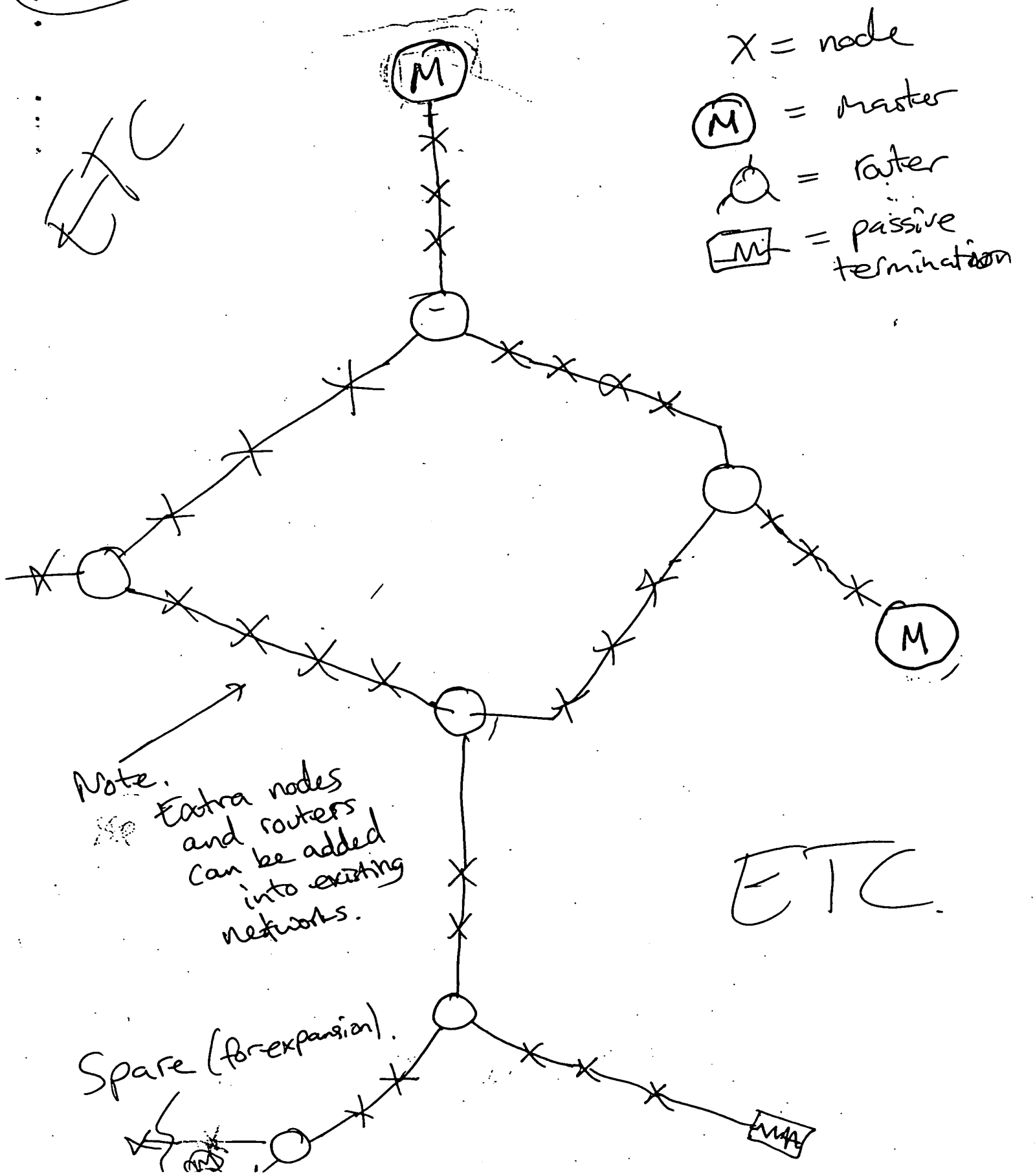
Capable of being addressed from both sides.
- Isolates two buses when reflecting to either.

FIG 14


Router
Symbol
B
A
C
Port B
R=Z0
Individual x3 Inductors.
D.C. or l.f. A.C. power input.
Z=Z0
Port A.
Port C.
Broadband Transformers x3 total
LOGIC BLOCK (STATE MACHINE).
A A B
C B C
(Route seled) outputs
Characteristic Z termination
Clocks
Datas
strobes
Reset
C B A
Signal
SIG
CLK DAT STR RES
3-level detection and timing detection

Complex Internet form



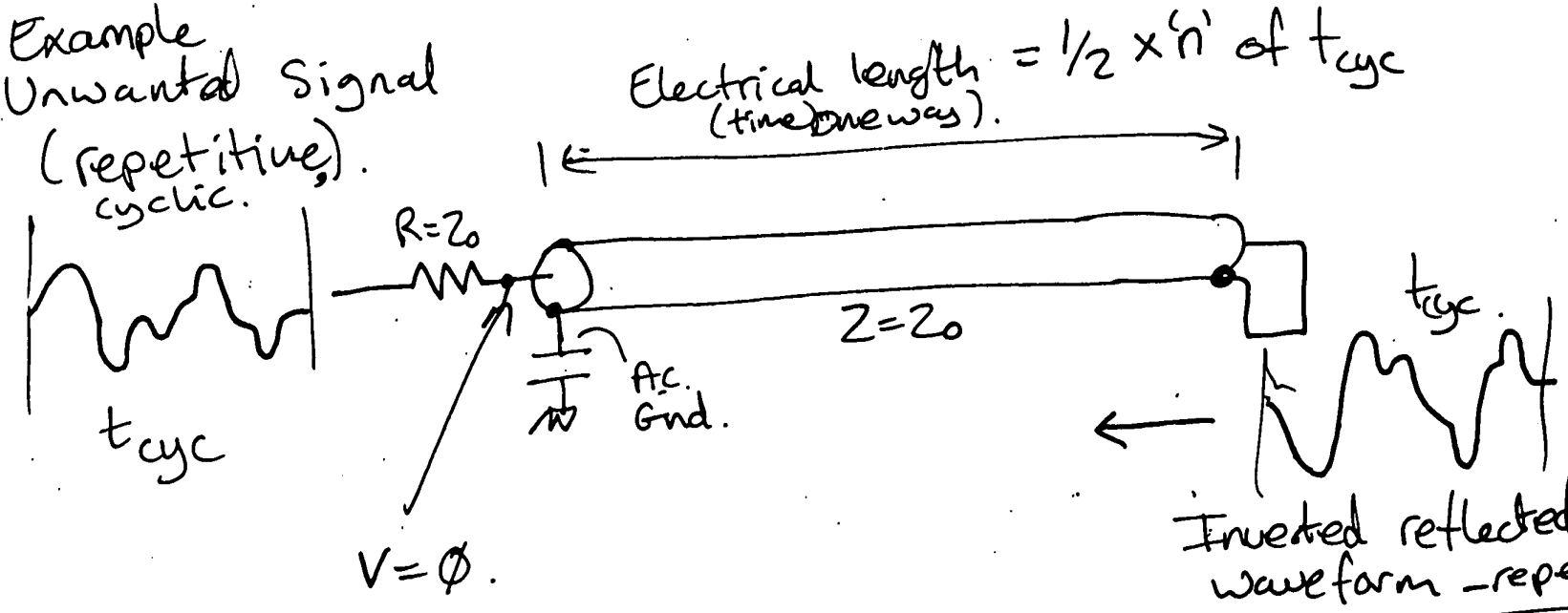


Reflection Rejection: Transmission Line (typ Coax)

F16b

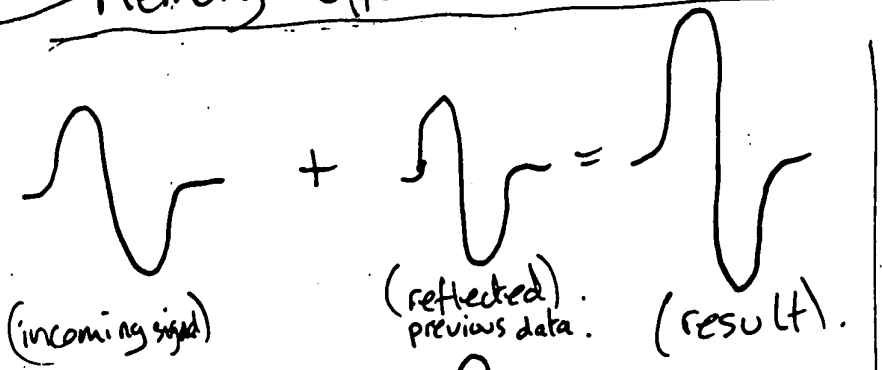
analogue 'Memory'

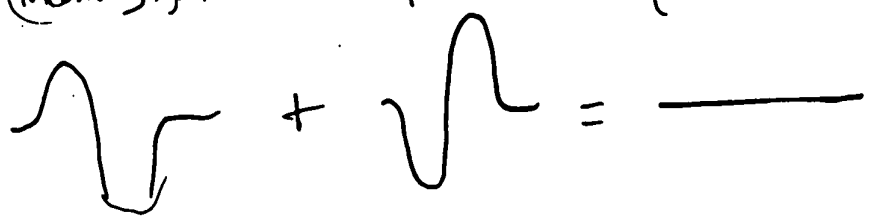
Example Unwanted Signal (repetitive, cyclic).

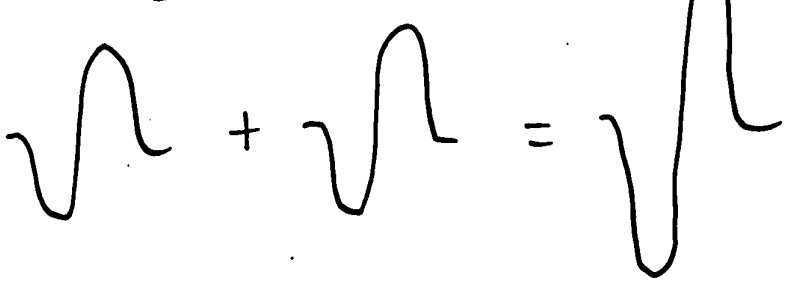


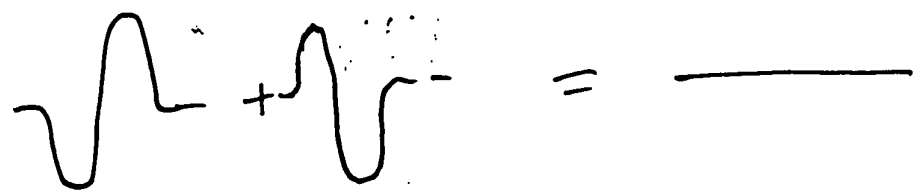
F16b

Memory effect on wanted signals when they combine. (Spurious signals having been removed)





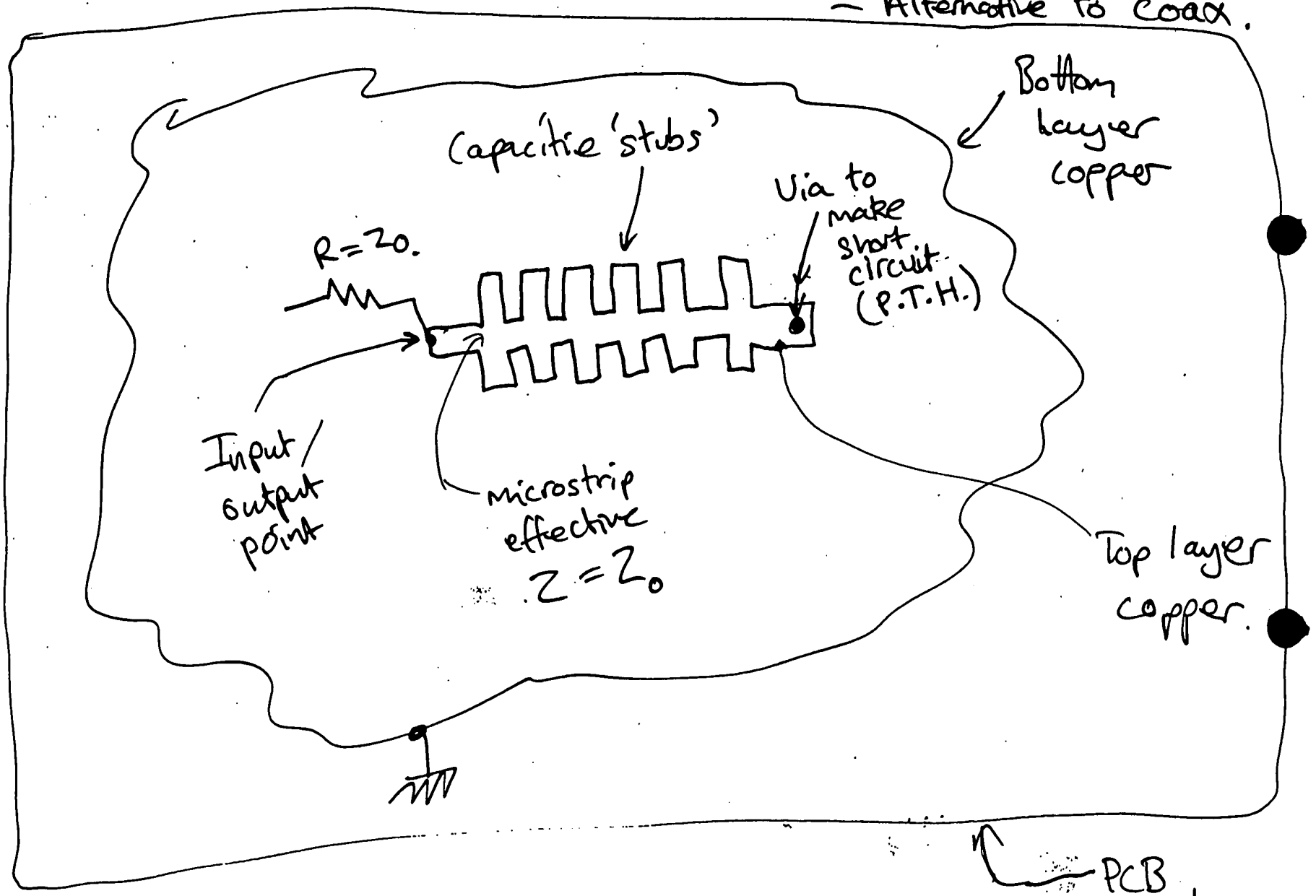




Microstrip (slow velocity) transmission line

'memory' for reflection elimination

— Alternative to coax.



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